1997 Advanced WORKSHOP ON FRONTIERS in ELECTRONICS

WOFE'97

Puerto de la Cruz,
Tenerife, Spain
6–11 January 1997

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The goal of this Workshop was to bring together leading scientists and engineers who are at the frontiers of electronic device and circuit research and development but who approach this technology for entirely different directions. The Workshop sessions included a Digital, Microwave, and Mixed Signal Session, an Optoelectronics Session, and a Future Direction Session. In addition to poster sessions, plenty of time was reserved for informal discussions and ad hoc poster sessions. This fostered a spirit of intellectual discourse, presented opportunities for the exchange of ideas and points of view, and hopefully gave the starting point for many future collaborations.

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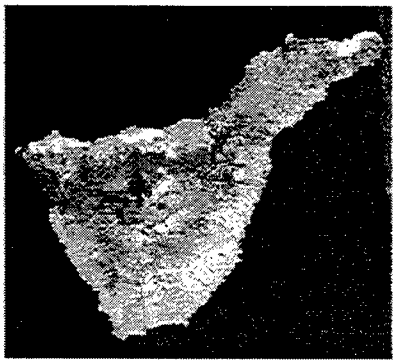

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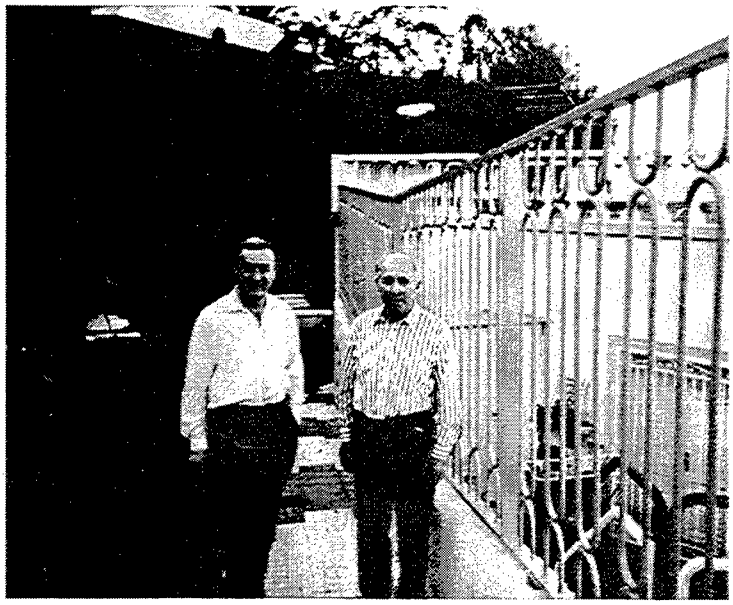

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PREFACE

The '*Advanced Workshop on Frontiers in Electronics*" (WOFE) was held at the Hotel Melia Puerto de la Cruz, Tenerife, Spain, January 6 - 11, 1997.

The goal of this Workshop was to bring together leading scientists and engineers who are at the frontiers of electronic device and circuit research and development but who approach this technology from entirely different directions. Low powered digital electronics, microwave powered circuits, and optoelectronics have become the foundation of today's electronics technology and seem to represent the directions for future endeavors, yet they emerged from traditionally separated fields and are still largely pursued by specialists trained in different areas.

The rapid pace of electronic technology evolution is propelling a merger of the traditional fields. Evidence is not hard to find around us. Wireless communication is just one example. It is time to encourage active cross-fertilization of the different "species" on this electronic planet and to call for leadership in bringing together the resources and expertise in these fields.

This advanced workshop was a special forum to gather some of the creative minds and leading experts from academia, industry, and government, and to review the most recent and exciting breakthroughs in the various fields, the underlying physical mechanisms that link these advancements , and to exchange views on future trends and directions, the market pulls and the necessary policy and infrastructure changes.

Not only different overlapping fields were represented at the Workshop but also different countries, including Canada, Great Britain, France, Germany, Iceland, Japan, Norway, Russia, Spain, and the U.S.

The Organizing and Program Committee worked very hard to assure a strong technical program. The invited speakers included Drs. Lester Eastman (US), Manfred Berroth (Germany), Didier Lippens (France), Frank Chang (US), T. P. Smith (US), Umesh Mishra (US), Clifton Fondstad (US), Serge Luryi (US), Jimmy Xu (Canada), Andrew Steckl (US), Manijeh Razeghi (US), J. R. Tucker (US), Hideki Hasegawa (Japan), Michael Dyakonov (Russia), T. C. McGill (US), Vidar Gudmundsson (Iceland), Elias Muñoz-Merino (Spain), and T. A. Fjeldly (Norway).

Dr. Paul Jay (Canada) organized a panel discussion on "Technology in 2007: Where Will It Come From?"

The Workshop sessions included a Digital/Microwave/Mixed Signal Session (chaired by Dr. Hans Rupprecht), Optoelectronics Session (chaired and organized by Dr. Y. S. Park), and a Future Direction Session. The workshop sessions served as the basis for organizing the proceedings into its four sections.

In addition to poster sessions, plenty of time was reserved for informal discussions and ad hoc poster presentations. This fostered the spirit of intellectual discourse, presented opportunities for the exchange of ideas and points of view and (we hope) gave a starting point for many future collaborations.

IEEE/EDS and IEEE/LEOS were technical co-sponsors of this meeting, which was made possible by generous financial support from ONR, ARO, ERO, EOARD, ONR-EUR, and NORTEL. This digest of extended abstracts will be widely distributed through conventional channels and through the Wide World Web.

Drs. Elias Muñoz-Merino and Pilar Aceituno provided invaluable help with local arrangements. They selected excellent facilities, interacted with local authorities, and were responsible for the social events, including the banquet, reception, and excursion.

We hope that the content and interaction offered at the Workshop will help all of us in determining the directions and approaches for our research for years to come. The proceedings offer a broader distribution of the ideas, results, and highlights of the meeting.

Gernot S. Pomrenke, Lead Editor and Publication Chair
Fritz Schuermeyer, WOFE Chair
Michael Shur, WOFE Program Chair
Jimmy Xu, WOFE Publicity Chair

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Digital/Microwave/Mixed Signal

Design, Fabrication and Characterization of GaN-based HFET's

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AlGaN/GaN modulation doped field effect transistors (MODFETs) with short gates show great promise for high power microwave amplifier applications. The lattice mismatch between $Al_xGa_{1-x}N$ limits the thickness and / or the fraction of Al in the barrier. An upper limit of x = .40 exists for 150 Å thick barriers for example, although lower x values and thicker barriers are commonly used. It is also possible to dope the channel, as well as the barrier, as will be presented later.

A simple analytical design model has been developed to show the tradeoff of 2DEG density with barrier composition and thickness, channel composition and thickness, and the location and sheet density of atomic planar doping. It assumes constant electron charge density in the channel, and uses the average potential in the channel for determining the 2DEG density. Barriers are placed on both sides of the channel. A design limit for the minimum barrier potential is .12 eV above the Fermi energy, to limit the barrier maximum probability of occupancy to .01. In terms of the 2DEG electron sheet density N_S, the potential variation ΔE_Q across the channel quantum well is

$$\Delta E_Q = \frac{qN_S}{\varepsilon_Q} \cdot a \tag{1}$$

where q is the electronic charge, ε_Q is the dielectric constant in the quantum well, and a is the half width of the quantum well. The potential variation ΔE_S across the spacer layer in the barrier is

$$\Delta E_S = \frac{qN_S}{\varepsilon_S} \cdot w_S \tag{2}$$

where ε_S is the dielectric constant in the barrier spacer layer, and w_S is the spacer layer thickness.

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The design location E_F of the Fermi level is

$$E_F = (\Delta E_C - .12\,\mathrm{eV}) - \frac{2}{3}\Delta E_Q - \Delta E_S \tag{3}$$

where ΔE_C is the conduction band potential step at the heterojunction. The two-dimensional density of states in each quantum well state is $8.8 \cdot 10^{13}\,\mathrm{cm^{-2}eV^{-1}}$ for the electron effective mass $m_e^*/m_0 = .21$ of GaN. Thus the 2DEG sheet density becomes

$$N_S = \left[(E_F - E_1) + (E_F - E_2) + \ldots\right] \times 8.8 \cdot 10^{13}\,\mathrm{cm^{-2}eV^{-1}} \tag{4}$$

where E_1, E_2, ... are the ground state energies for the $n = 1, 2, \ldots$ quantum well states. Only those states whose ground state is below the Fermi level are included. For narrow quantum wells, the electrons can be all in the $n = 1$ state, yielding good mobility. Substituting (1) and (2) in (3), and solving simultaneously with (4) yields the maximum value of N_S with limited electrons in the barrier. ΔE_C is made large by using an $Al_xGa_{1-x}N$ barrier with high Al fraction x, and $In_yGa_{1-y}N$ quantum well with high In fraction y. in both cases, x and y are limited by the Matthews-Blakelee pseudomorphic limit. Using x = .4, y = .35 and a 50 Å spacer, a 30 Å InGaN quantum well, the system yields $N_S \cong 5 \cdot 10^{12}\,\mathrm{cm^{-2}}$. A complete quantum mechanical solution using the Cornell computer program CBAND normally yields N_S ~ 10% higher in value.

Most GaN has a high density of dislocations, threading through the epitaxial layer. A model that assumes that dangling bonds are acceptors, at ~ 2.2 eV below the conduction band, was used to predict the electron mobility as a function of donor concentration and dislocation density. It showed that the mobility maximized, at a specific donor density, for each dislocation density. For 10^8, 10^9, 10^{10} $\mathrm{cm^{-2}}$ dislocation density values, the maximum bulk mobilities (parallel to the surface) that are expected are 1600 $\mathrm{cm^2/Vs}$ (at 10^{15} $\mathrm{cm^{-3}}$ doping), 825 $\mathrm{cm^2/Vs}$ (at 10^{16} $\mathrm{cm^{-3}}$ doping), and 340 $\mathrm{cm^2/Vs}$ (at 10^{17} $\mathrm{cm^{-3}}$ doping), respectively.

These dislocations are usually perpendicular to the surface, and thus yield potential spikes that scatter electrons in the MODFET 2DEG. For high electron sheet density values, and thus higher Fermi energy levels, the scattering from dislocation ions, as well as from remote ions in the barrier, will be reduced, yielding higher mobility.

Two HFET material designs were prepared on sapphire substrates and tested with short gates. The first one was a MODFET with a 75 Å GaN channel and with $Al_{.16}Ga_{.84}N$ barriers on both sides. There was a 20 Å thick, $2 \cdot 10^{18}$ $\mathrm{cm^{-3}}$ doped barrier layer, removed from the channel by a 50 Å spacer layer. A top cap layer, 10 Å thick, was also Si doped and had $Al_{.06}Ga_{.94}N$ composition. The total barrier thickness from the Schottky gate to the

channel was 260 Å. The electron sheet density was $7.3 \cdot 10^{12}$ cm^{-2}, and the mobility was 680 cm^2/Vs. This sheet density is higher than predicted, possibly due to piezoelectric effect. A .25 μm × 100 μm MODFET yielded $f_T = 21.4$ GHz, and $f_{max} = 77.45$ GHz. The effective gate length is approximately .31 μm, after considering fringing fields toward the source and drain, limiting f_T. The gate pad capacitance also limits f_T. The knee voltage for $V_{gs} = 0$ was about $V_{ds} = 7$ V, yielding about 150 mA/mm, both affected by the 10 Ωmm source resistance. Operation to 10's of volts on the drain was possible at low drain current.

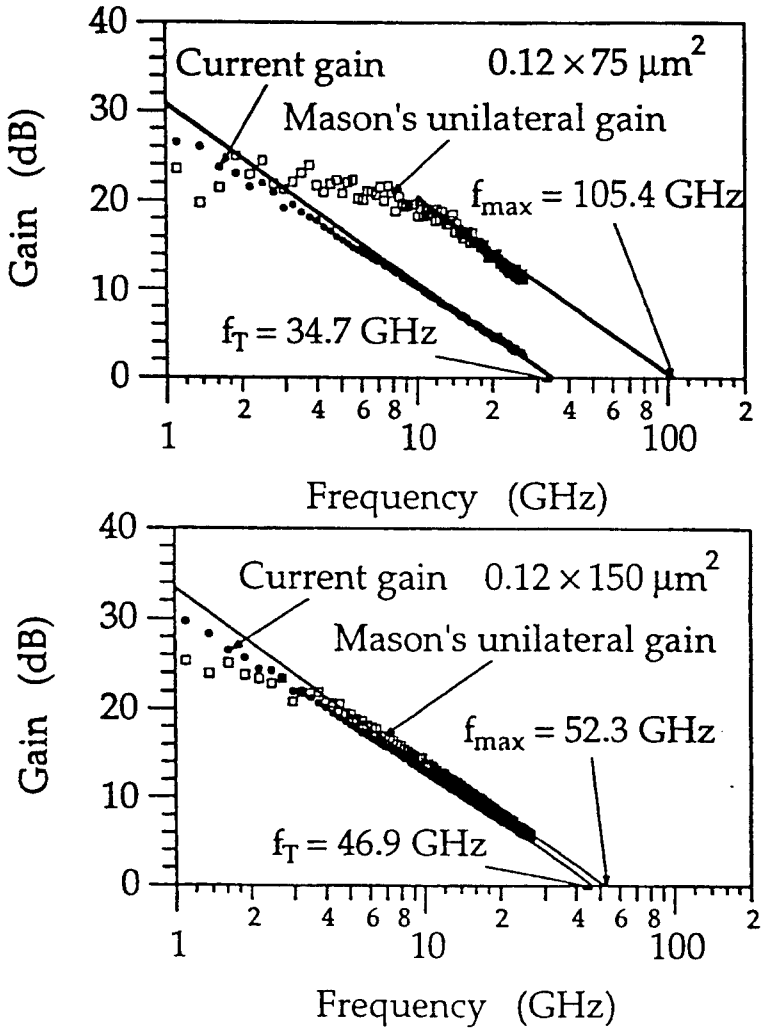

figure 1: MODFET frequency response for different device geometries

The other structure had a .1 μm GaN doped channel, a barrier of $Al_{.15}Ga_{.85}N$, with a 30 Å undoped spacer layer between the channel and the doped part of the barrier. The doped part

of the barrier was 300 Å thick. The physical gate length was .12 μm, but the effective gate length, when half of the channel was depleted, was estimated to be .285 μm due to fringing gate fields. Devices with 75 μm and 150 μm periphery yielded f_T values of 34.7 GHz and 46.9 GHz, respectively, as shown in figure 1. Plotting $1/f_t$ vs. $1/w_g$, where w_g is the gate periphery, allows an extrapolation to yield the intrinsic f_{Ti} by eliminating the effect of the gate parasitic capacitance. The f_{Ti} value is 72.4 GHz, which in turn yields ~ $1.3 \cdot 10^7$ cm/s average electron transit velocity for an effective gate length of .285 μm.

In the latter device, source contact resistance was improved to the range of 4...8 Ωmm, which is still large enough to limit the maximum drain current and the g_m. Drain current of 550 mA/mm and g_m of 110 mS/mm were achieved, with ~ 5 V knee voltage, at $V_{gs} = 0$. At high operating frequency the contact resistance is largely bypassed by the parallel capacitance, allowing high f_T and f_{max}. The f_{max} values for the 75 μm and 150 μm periphery devices were 105.4 GHz and 52.3 GHz, respectively.

A key attribute of GaN HFET's is the very high drain-source breakdown voltage, even with short gates. Values ranging from 50...100 V with the .12 μm gate length devices were measured. These values are about ten times those for GaAs MODFET's, allowing for ten times as much power per mm of periphery. In addition, the optimum load impedance is ten times higher, allowing ten times the periphery for a given load impedance. In order to handle the higher level of power, SiC substrates, with ten times the thermal conductivity of GaAs, must be used. For a 100 μm thick SiC substrate, the thermal resistance is ~ 10 °mm/W. Such SiC substrates will be Vanadium doped to have semi-insulating properties.

In summary, AlGaN/GaN HFET's with short (.12 ... .25 μm) gates have been fabricated both with and without doping in the channel. An average electron transit velocity was deduced to be $1.3 \cdot 10^7$ cm/s for .12 μm gate doped channel devices. Extrinsic f_T as high as ~ 47 GHz, and extrinsic f_{max} as high as 105 GHz were obtained with .12 μm gate devices with 150 μm and 75 μm periphery values, respectively. A simple analytical model, generally useful for designing MODFET materials has been presented. The results of a model to predict mobility of electrons in the presence of charged dislocations were also presented. Finally, the prediction of obtaining up to ten times as much power per millimeter, at ten times as high an optimized load impedance, when compared with GaAs pseudomorphic MODFET's, is made.

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RF Power Potential of HEMTs

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The growing demand for mobile communication is not only driven by hand-held phones. Wireless local area network and personal digital assistants are also requiring high frequency power amplifiers with high power added efficiency. Even higher frequencies of operation are required for base station interlinks and sensor applications like automotive collision avoidance radar.
Several watts of output power at millimeter wave frequencies is a very demanding target with the high electron mobility transistor (HEMT) as the most promising candidate. In this paper the present status of millimeter wave transistors and circuits as well as future applications will be discussed.

I. Introduction

The availability of solid state amplifiers will encourage new applications at millimeter wave frequencies. There are various frequencies used in the frequency range between 25 and 50GHz for communication links. The required power is often well above 1 Watt, which is still state-of-the-art for monolithic integrated circuits at these frequencies. These base station interlinks do not have the market potential of other applications like intelligent cruise control with a millimeter wave radar sensor. As low cost is a requirement for this automotive application, a single chip frontend will be a very demanding target for the semiconductor supplier. Similar demands will arise from active phased array radars in the W-band for defense applications. The reduced antenna dimensions are also restricting the volume of the transmit/receive modules, which is minimized by single chip solutions. Therefore not only the power density of transistors at millimeter wave frequencies has to be improved, but also matching and power combining design methodologies.

II. HEMT Performance

The transistors with best power performance at millimeter wave frequencies are pseudomorphic HEMTs either on InP or GaAs. The RF performance can be described with current gain cut-off frequency f_T and maximum frequency of oscillation f_{max}. Applications at V- or W-band require transit frequencies well above 100 GHz and f_{max} at about 200 GHz. Those figures of merit can only be achieved with a transistor gate length of about 0.1 µm as predicted with the saturated velocity model:

$$f_T = \frac{v_{eff}}{2\pi l_g}$$

As the saturation velocity has the same order of magnitude of 10^7 cm/s for most semiconductors, the submicron gate length is a prerequisite for W-band solid state amplifiers based on FETs.
The maximum frequency of oscillation can be estimated neglecting the feedback capacitance and other parasitic resistances by the following equation [2]:

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$$f_{\max} = \frac{g_m}{2\pi C_g \sqrt{\frac{4(R_S + R_G)}{R_{DS}}}}$$

We can see that low parasitic source and drain resistances R_S and R_G as well as a high output resistance of the transistor are determining f_{max}. This relationship has several implications to the fabrication process. The gate recess reduces the source resistance by a highly doped cap layer. The gate resistance is reduced by mushroom gate profile. The output resistance can be increased by improving the confinement of the electrons in the channel. Therefore higher conduction band offsets on both sides of the channel will improve high frequency performance.
The maximum high frequency output power of the transistor can be estimated from the IV-curves of the transistor. An optimum load line is matching the maximum drive current at low drain voltage with the breakdown voltage close to pinch-off. The output power is limited by the following formular:

$$P_{out} = \frac{1}{8} I_{DS\max} U_{BV}$$

For a given operating voltage we have to maximize the charge carrier density, i.e. optimize the layers of the heterostructure in respect to doping concentration, their distribution as well as material composition. In general increasing the doping results in a decrease of breakdown voltage. This can be described for the MESFET with the following equation [3]:

$$U_{BV} \propto \frac{1}{\int_0^d N(y)dy}$$

N(y) is the doping distribution and d is the total channel thickness. Therefore the breakdown voltage-saturation current product does not change a lot. The resulting power transistor structure is a pseudomorphic double heterojunction (DH) HEMT with current densities of about 1 A/mm and breakdown voltages of a few volts [4]. This limits the power density well below 1 W/mm at millimeter wave frequencies. Recent simulations show that doping in the channel will improve the output power of the DH HEMT [5]. The ultimate limit to this optimization process was already given by Johnson [6]:

$$\sqrt{P_m X_c} f_T = \frac{E_c v_{sat}}{2\pi}$$

The output power is limited by the dielectric breakdown field E_c and the saturation velocity of the charge carriers v_{sat} and decreases with increasing transit frequency. At high frequencies the switching losses have to be taken into account as well. Baliga [7] has derived a high frequency figure of merit, which can be estimated for MESFET type structures from material parameters:

$$f_B = \frac{1}{R_{on}' C_G'} \approx \mu E_c^2 \sqrt{\frac{U_G}{4U_{BV}^3}}$$

This relation indicates that the power losses in the device can be reduced by increasing the mobility of the charge carrier supporting the superiority of HEMT's for high frequency power applications.
These considerations however do not reflect the limitations of other parasitic external elements of the device. As already discussed for the maximum frequency of oscillation, the source and gate resistances are limiting the high frequency performance of the transistor. With increasing transistor width the source resistance as well as channel on-resistance are decreasing while the gate capacitance increases and keeping f_B constant. The gate resistance however increases with transistor width limiting f_{max} as well as the RF output power of a single finger device. The

optimum transistor size given by the Baliga high frequency figure of merit is therefore not feasible and the single finger width is determined by gate resistance and the required output power has to be achieved by connecting n transistor fingers in parallel.

III. Design Considerations

For millimeter wave applications there arises a severe design problem by combining many transistor fingers for high power amplifiers. At 100 GHz the wave length on GaAs substrate is about one mm using coplanar or microstrip transmission lines. The high frequency path to and from any single transistor finger from input to output has to be matched for all possible paths better than 1/10 of the wavelength for efficient power combining. Using conventional 1:n power divider and combiner structures with symmetric layout for input/interstage and output matching huge die areas are wasted for simple metal structures without an active device on the expensive epitaxial grown wafer.

To minimize die size and increase output power new design concepts for interstage and output matching should be investigated. Instead of discrete large trees of 1:2 dividers to achieve the 1:n ratio more distributed structures as well as quasi-optical methods should be considered.

The distributed structures may be similar to the recently proposed transmission gate FET for distributed amplifier design, which uses the single finger transistor as part of the input matching network [8]. This should be enhanced for transistor arrays with minimized area consumption for passive matching structures. The modeling of those amplifiers might require distributed models for the passive structures and even for the transistor fingers.

Another approach could be a linear array of transistors forming a loaded transmission line for the input as well as the output network. This concept would copy the traveling wave tube to semiconductor amplifier.

The low losses of discrete quasi-optical power divider at millimeter wave frequencies is encouraging the investigation of quasi-optical passive structures also for monolithic integrated circuits. This would also include antenna arrays on-chip for quasi-optical power combining off-chip.

Due to the high losses for every transition from one chip to the substrate or from chip to chip the monolithic integration of the whole RF frontend is anticipated. The millimeter wave phased array radar is a good example of the present research problems [9]. To achieve the required output power, the above mentioned problems arise. The monolithic integration of the transmit/receive module on a single chip not only minimizes chip size by avoiding transition losses, but also matches the demanding volume restrictions of the small millimeter wave antennas when each of the antenna elements is fed by a T/R chip. Especially space or airborne systems require minimum size and weight at high power efficiency.

IV. Conclusion

The millimeter wave output power of semiconductor devices and circuits is not limited to present levels of about 1 watt. Material and process optimization will increase the power density of the individual device, while improved combining structures will increase the total output power of millimeter wave amplifiers. This will allow very compact antenna and system designs as required for space or airborne systems.

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Challenging issues of quantum devices

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Abstract: Quantum effects concern carrier localization, tunneling and interference effects. They give rise to remarkable conduction properties notably negative differential conductance, special symmetry and directivity. In this paper, two classes of structures will be more specially addressed involving either a lateral or a vertical transport in semiconductor heterojunctions. For the electron waveguides representative of a lateral transport, I will focus on the necessary conditions for a high directivity in multi-port devices by means of interference patterns or symmetry breaking. For the second kind of structure, special attention will be paid to resonant tunneling structures in two-terminal configuration. Beyond the search of an efficient control of resonant tunneling currents, I will report on figures of merit notably for ultra-fast analog applications.

1. Laterally confined geometry:

In this section, I am dealing with electron waveguides starting from a high electron mobility modulation doped heterostructure. A gate pattern implemented on top of this heterostructure has made it possible to control the lateral extent of a two-dimensional gas at the hetero-interface thus creating lateral confinement potentials which can be described in a first approximation as parabolic walls. Furthermore, if the length of these quasi one-dimensional microstructures is less than the phase coherence length over which the electrons retain phase information, the transport is ballistic. Under these conditions, these *laterally confined* structures behave as electron wave guides with conduction properties solely determined by the geometry of systems [1]. In connection with conduction properties, well known plateau-like structures are obtained in the conductance-voltage characteristics due to transverse quantum effects. Moreover stub-like configuration can be used for modulating the transmission[2]. At this stage, I will focus on multi-port structures which offer further degree of freedom in the design with a generic structure which can be compared to a microwave coupler. Such a device was successfully fabricated with a tunneling coupling barrier[3]. Here I will focus on the various possibility afforded by open coupling windows with single and dual coupling branch schemes.

As a first example, let us considered the structure depicted in the inset of figure 1 and whose conductance (G) characteristics versus wire width (Lw) are reported in the same figure. The numerical procedure for calculating G was detailed in reference [4 b]. For comparison, we also reported the variation of conductance for a uniform wave guide. With respect to this situation, it can be seen that a high transmission is obtained towards port 4 for Lw around 20nm. This is the typical situation of a backward wave regime where a quasi full transfer occurs between the two parallel waveguides along with a reversal in the direction of propagation. In order to have a better understanding of this turn around process, figure 2 shows a three-dimensional plot of the modulus of the wave function $|\Psi|$. It exhibits a node in the two quantum regions connecting ports 3 and 4. Such a pattern is characteristic of a two-order mode which cannot propagate in the quantum wires owing to cut-off considerations. This explains the rapid evanescence of the probability waves in these two output ports. On the other hand, it can be seen that the wave function is highly asymmetric in the coupling branch with an accumulation in the presence probability density close to the confinement wall located on the right hand side of the figure. This symmetry breaking was a key feature for a successful backward operation.

Another frequent use of couplers is the so-called "hybrid" (3dB) coupler where the incident stream is equally shared between two of the three output ports [4a]. Such a configuration can be obtained by the use of a double branch coupler (DBC) with characteristic dimensions for the wires and for the interaction region of the same order preserving by this means a monomode operation.

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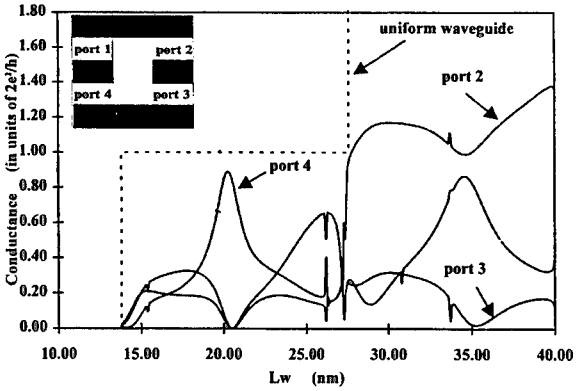

Figure 1 Conductance characteristics at the output ports as a function of Lw (single branch coupler)

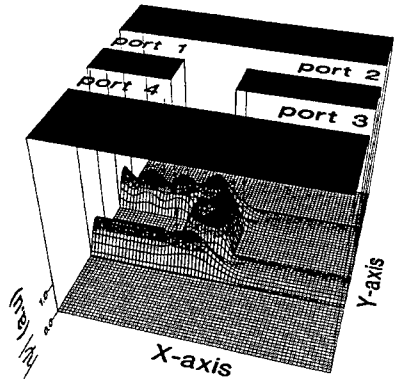

Figure 2: illustration of a backward operation

In order to illustrate the mechanisms involved in such a structure, figure 3 gives the two dimensional plots of the probability density for a 3 dB coupling. It can be seen that an equal sharing of the presence probability is apparent at the output ports 1 and 3 along with a low reflection coefficient at the feeding port 1 (quantitatively lower than 0.01). In contrast, the probability at port 4 is very low attesting of a high directivity in the electron stream control (17 dB). Such effects are a direct consequence of the two distinct coupling paths and one can expect that the electron waves are in-phase in the sub-region near port 3 and out-of-phase in the vicinity of port 4. This interpretation based on constructive and destructive interferences can be supported by analyzing the iso-phase pattern. It can be demonstrated that the two branches behave differently with well defined phase rotation for the second branch whereas the phase in the first branch is almost constant. The fact that the phase front is lost for the latter can be explained by the superimposition of a primary electron stream transmitted by the first coupling branch and a back-scattered wave issued from the second branch. On the other hand, It can be shown that these transfers of charge are very fast, on subpicosecond time scale and can be used as a quantum interference electronic switch [4c].

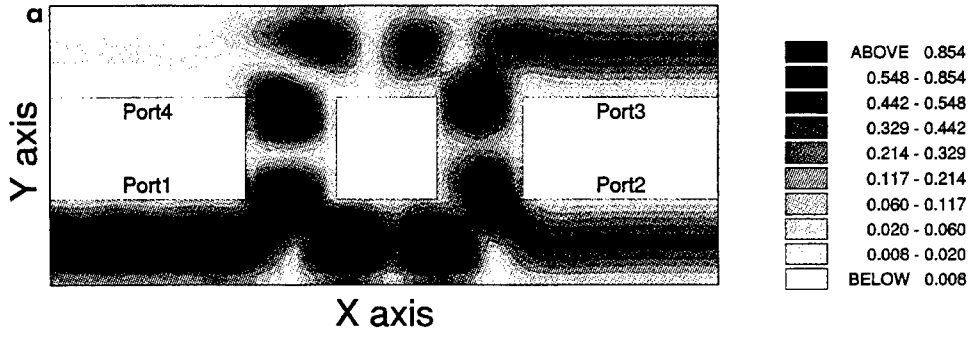

Figure 3:Two-dimensional view of the modulus of the wavefunctions for a 3dB coupling operating mode using a double branch scheme. Reference energy is 31 meV. Dimensions are 20 nm.

3: Vertically confined geometry:

For quantum interference device, briefly discussed above, a number of limitations in the present state of technology can be pointed out including a degradation of performances for a multimode operation, a poor temperature robustness and more importantly a low current drivability. The double barrier heterostructure (DBH) which takes advantage of a resonant tunneling effect via the quasi-bound states of a quantum well does not suffer from these drawbacks [5]. From this view point, it appears as one of the most promising development at short term involving nonlinear electronics [6] and high functionality digital circuits[7].

In the following, I will focus on the various means to optimize two important figures of merit which are the peak current density (Jp) and the peak-to-valley current ratio (PVR). To this aim, let us consider the main guide lines for the choice of the material system. Clearly the quantum transmission through the barrier is greatly reinforced provided that the effective mass is low and the barrier ultra-thin. For the former, there still exists an uncertainty about the effective tunneling mass which governs the evanescence of the electron wave within the barrier but low gap (low effective mass) adjacent layers appear generally preferable. The shrinking in the barrier thickness is limited at about 1nm due to interface roughness on monolayer scale. Under these conditions, current density in excess of 100 kA/cm^2 can be expected [8]. Also of major concern is the peak-to-valley current ratio which is decreasing at increasing Jp. This trade-off results directly from the strong coupling of the semiconductor resonant cavity with the contact regions, of prime importance for a high current drivability.

On the other hand, it can be shown that a pure coherent tunneling situation is no longer valid with scattering-assisted tunneling paths which reduce drastically the PVR. Nevertheless, the performances exhibited nowadays by resonant tunneling diodes are quite impressive in terms of peak current and current contrast. In order to illustrate this issue, I reported in figure 3 the dc characteristics, we recently obtained [9] for an intra-band pseudomorphic InGaAs/AlAs resonant tunneling diode epitaxially grown on InP substrate. Here PVR exceeds 6:1 for a peak current density up to 175 A/cm^2 for a 1.4 nm barrier thickness which compare favorably to the best results reported so far.

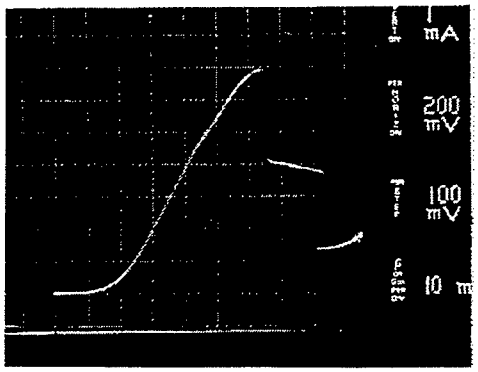

Figure 4: dc characteristics for an intraband tunneling structure
(Strained InGaAs/AlAs DBH diode)

To further increase the current contrast, several ways are usually employed with notably InGaAs perturbations [10] which permits a large energy offset between ground and excited quantum states. Another elegant way is to use antimonide based material systems with unique features in terms of interband tunneling phenomena [11]. Up to now, InAs/AlSb/GaSb resonant interband tunneling diodes (RITD) are particularly representative of these studies on this material system which exhibits an overlap under equilibrium between conduction and valence states. For illustrating this issue, the conduction and valence band profiles, we calculated recently by means of a two-band model, are reported in Figure 5 for a typical Sb-based RITD. Heavy holes accumulates within the GaSb quantum well whereas it can be demonstrated that the current contribution is

dominated by the resonant transmission of light holes via the quasibound states of the quantum well. The potential advantages of such a structure are clearly apparent in this figure with practically no conduction threshold and an expected large PVR when the band gap of GaSb prevents any leakage current through the structure. This high PVR was demonstrated. However to the best of my knowledge, the highest current density reported so far was 75 kA/cm^2[12], often sufficient for digital applications, but well below the state of the art for intraband tunneling structures.

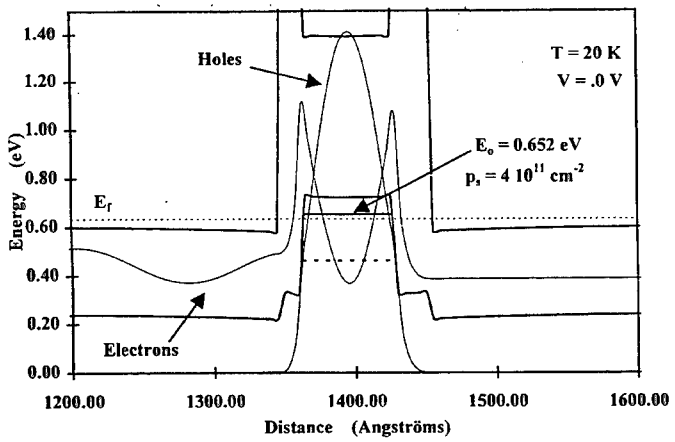

Figure 5 Energy profile for an Sb-based double barrier heterostructure (InAs/AlSb(1.5nm)/GaSb(6.5nm)/AlSb(2.5nm)/InAs)

5. Conclusion:

In this short overview of key features of some quantum devices including resonant tunneling diodes and electron wave guides, we learned that unique conduction properties can be achieved by taking advantage of interference, localization and tunneling effects. A high directivity in the control of electron streams was found for four-port electron waveguides with full electron transfer or equal sharing of waves. For resonant tunneling diodes extremely high current density can be obtained by means of strained layer epitaxy and the tremendous flexibility of antimonide based material system can be used for improving the peak to valley current ratio when carriers experience the forbidden states of Sb-based material. For both types of devices, subpicosecond dwelling times in the active region can be found and it is believed that this new class of devices can find applications in low power consumption and ultra-fast applications notably at terahertz frequencies.

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HETEROJUNCTION BiFET TECHNOLOGY FOR HIGH SPEED ELECTRONIC SYSTEMS

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Abstract

A GaAs BiFET LSI technology has been successfully developed for high speed, low power and mixed signal circuit applications. The direct placement of the FET on the HBT emitter cap layer simplifies the device epitaxial growth and process integration. High integration levels and functional circuit yield have been achieved. Excellent HBT and FET characteristics have been produced, with the noise figure of the FETs comparable to those of traditional MESFETs, enabling them to perform well in front end receiver applications. Through this technology, several LSI circuits, including a 2 Gsps 2–bit prototype DRFM, 2 GHz 32 × 2 bit shift registers, sample and hold circuits with 9–bit resolution at 200 Msps and SRAMs with ultra-fast access time (330ps) have been successfully demonstrated.

Introduction

The integration of GaAs HBTs and MESFETs (called Bipolar/FET or BiFET) can make a significant impact on the design of high performance and mixed signal integrated circuits and systems. BiFET technology offers great design flexibility and novel circuit opportunities by combining the device advantages of the HBT's high switching speed, high drive capability, excellent threshold voltage matching, and low 1/f noise; as well as the FET's low noise, high input impedance, high density, and low power dissipation on a single chip. In particular, the addition of MESFETs provides active loads, low voltage currents sinks for minimizing power consumption, and floating current sources to provide high gain.

Previously reported demonstrations of HBT/FET integration,[1-3] involving the selective area regrowth or the use of collector layer for the FET, have not advanced to the point of useful circuit integration. To achieve high integration levels and high yield, a planar BiFET IC process[4,5] has been developed with only two extra masking layers (FET gate and source drain ohmic layers) added to an HBT process and using commercially available MOCVD HBT wafers. The developed fabrication technology has several advantages over other integration approaches for HBTs and FETs. The most obvious one is the use of the already existing emitter epilayer (Figure 1) to define the FET active channel. This eliminates the need for material regrowth (the entire structure is grown in a single epitaxial sequence), provides a more planar structure, and avoids the need of forming p-type buried layer to reduce both short channel and sidegating effects.

To demonstrate the producibility and versatility of the developed BiFET technology, various LSI circuits such as a wide bandwidth single chip Digital Radio Frequency Memory (DRFM), high speed SRAMs and high resolution sample/hold circuits have been successfully fabricated and tested.

Device Structure and Fabrication

The BiFET process developed at Rockwell uses commercial MOCVD HBT epitaxial wafers on a semi-insulating GaAs substrate. A lightly doped GaAs emitter cap layer (1000Å, 5-8 x 10^{17}/cm^3) is inserted between the lightly doped AlGaAs emitter (700Å, 5 x 10^{17}/cm^3) and heavily doped GaAs emitter cap layer (500Å, 5 x 10^{18}/cm^3. A thin highly carbon-doped GaAs base layer (500Å, 4 x 10^{19}/cm^3) and lightly doped GaAs collector layer (7000Å, 3 x 10^{16}/cm^3) are used for HBTs. The heavily doped GaAs emitter cap layer can be replaced by InGaAs to facilitate a refractory metal contact. The typical material growth sequence and layer structure of the HBT are summarized in Figure 1.

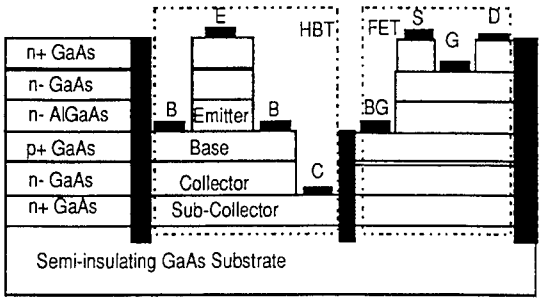

Figure 1. Schematic cross section of the monolithic integrated GaAs HBT and MESFET.

The FET was fabricated from the emitter cap epilayers. During normal operation of the FET, the AlGaAs layer in the HBT emitter is fully depleted; thus the conduction paths remain primarily in the GaAs (rather than lower mobility AlGaAs) apart from real space transfer of electrons. The FET ohmic was on the heavily doped emitter cap layer. The backgate (BG) is a unique feature of the FET, which was formed on the p+ GaAs during the same fabrication process of the HBT base contact. Like the front gate, the backgate can also be used to modulate the FET channel. Gate recessing was performed using an $NH_4OH:H_2O_2:H_2O$ wet chemical etch with the end point determined by monitoring the channel current. Several steps in the MESFET fabrication process have been combined with the HBT process, including ion implantation for device isolation and all metalization for interconnects. A standard baseline non self-aligned HBT process was implemented for the device and circuit fabrication.[7] In this process a Schottky diode was formed on the collector layer; thin film NiCr resistors were also fabricated. The interconnects were processed along with the HBTs using standard Ti/Au metalizations and polyimide for intermetal isolation. All of the process steps are identical to a standard HBT, with the exception of the gate definition.

BiFET Device Performance

The HBTs fabricated in this technology are comparable to those of our standard non self-aligned HBT process. I-V characteristics are shown in Figure 2. Good current gain (> 50 at 1 mA) (Figure 2) and excellent RF properties (f_t and f_{max} > 50 GHz at Ic = 3 mA) have been achieved for a 1.4 × 3 μm^2 device. This process has also produced both E-mode and D-mode MESFETs with excellent characteristics on an HBT structure. Typical I-V characteristics for an enhancement-mode (normally off) MESFET fabricated on the HBT emitter cap with source grounded to the backgate are shown in Figure 3. The uniformity of the threshold voltage is about -0.90 ± .05 V for D-FETs and +0.1 ± 0.03 V for E-FET. The threshold voltage of the FET can be altered by applying a bias to the backgate as shown in Figure 4. MESFETs with

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submicron gates (0.5 μm) have been fabricated by using optical lithography and a substitutional gate process. The f_t and f_{max} of FETs were measured to be 40 and 35 GHz (Figure 5), respectively; the g_m of the FETs ranged from 250 to 350 mS/mm. The fabricated 0.5 μm gate FETs also have comparable noise figures (a 1.8 dB noise figure and 8 dB associated gain at 10 GHz and a 1.2 dB noise figure and 19 dB gain at 1 GHz) to that of regular MESFETs with the same gate length. Further reduction in the gate length will result in significant improvement of f_t, f_{max}, and the noise performance of the FET.

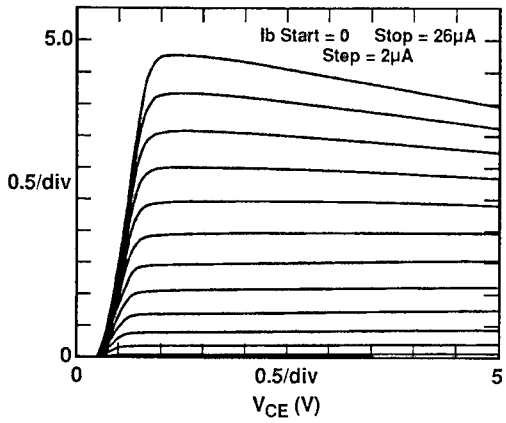


Figure 2. I-V characteristics of (a) GaAs HBTs with emitter dimension of 1.4 μm × 3 μm.

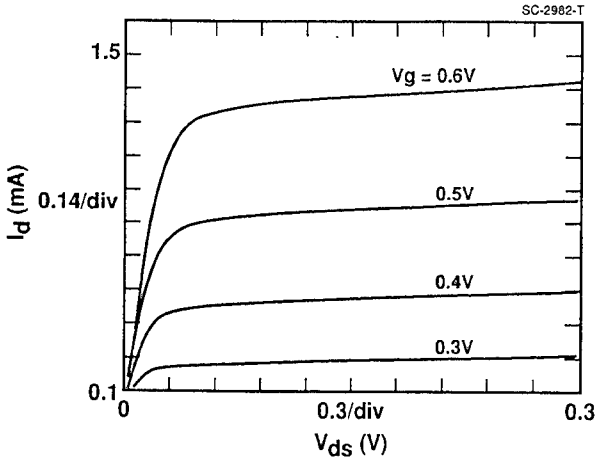


Figure 3. I-V characteristics of GaAs MESFETs with gate length of 0.5 μm fabricated in the BiFET process.

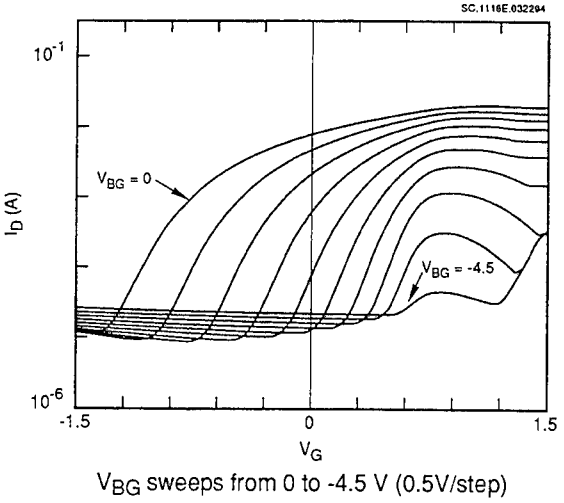


Figure 4. Threshold voltage vs applied backgate voltage.

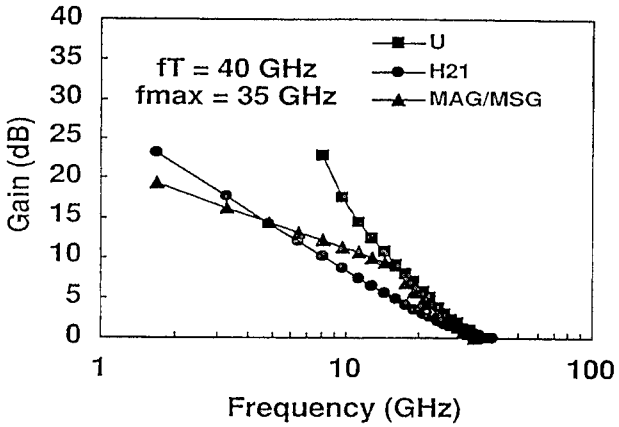


Figure 5. Gain vs. Frequency for FETs with 0.5 μm gate length fabricated on HBT emitter epilayer.

Circuit Demonstrations

Several key GaAs BiFET circuits have been demonstrated. Those include the first LSI circuits: a single chip prototype DRFM, 32 x 2-bit word shift registers, 200 Msps sample/hold circuits and ultra-fast SRAMs.

DRFM on a Single Chip

The fabricated DRFM (Figure 6) consists of a 2-bit ADC, a 2-bit DAC, 32 x 2-bit word shift register and supporting circuitry. It contains 518 HBTs, 1572 FETs and 332 Schottky diodes. The DRFM system diagram is shown in Figure 7. The designed system can be easily expanded in both length and width. Basic functionality consists of digitizing an input signal through a 2-bit analog to digital converter (ADC), selectively delaying (or storing) the pattern by using a 32 x 2-bit word shift register, and then reconstituting it with a 2-bit DAC. Full functionality (Figure 8) was achieved with yield over 50% on the best wafer. The DRFM was also found to be operational up to 2 GHz.

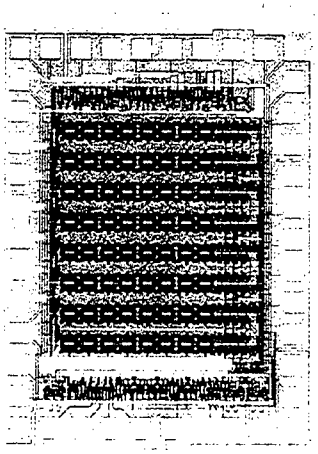


Figure 6. Microphotograph of a fabricated BiFET DRFM.

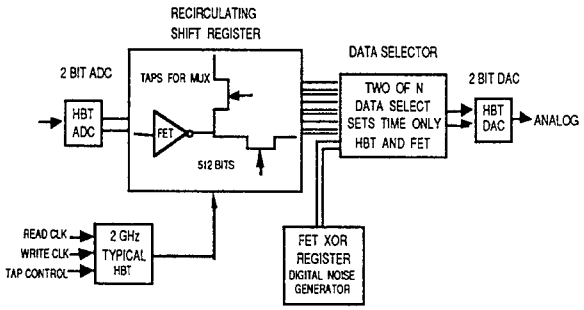
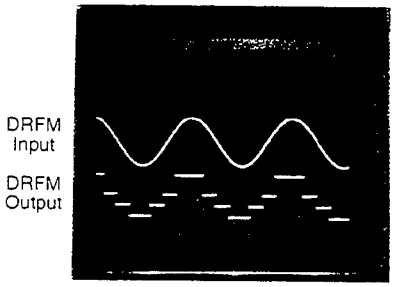
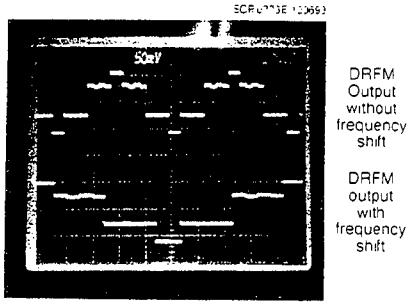


Figure 7. DRFM system diagram, which consists of a two–bit ADC, a two–bit DAC, a 32–bit by 2–bit word shift register, and support circuitry.



(a)

Figure 8. (a) DRFM output waveform, (b) Input signal frequency down shifted by 2–bit DRFM.



Input frequency shifted
by 2-bit DRFM

(b)

Figure 8 (Continued)

32 x 2–bit Word Shift Register

Two different logic types of a 32 x 2–bit shift registers (Buffered HBT Logic (Figure 9) and Buffered FET Logic) were also demonstrated on separate chips. The circuits consist of 4-bit long by 2–bit wide shift registers with input data multiplexers, which allow data to be selected from two different sources. Eight of these 4–bit shift registers are required for the 32–bit version. The basic building block for the shift register is shown in Figure 10. The circuit uses an HBT for good drive, floating current source MESFET as the pullup, and obtains additional level-shift from the HBT. The gate topology was chosen for robustness to process variations, but E–D or dynamic logic can be used to enhance its speed-power performance. The shift registers serve as the data storage for the DRFM and allows the signal to be captured and read out repeatedly. Shift registers were fully functional (Figure 11), with 80% yield on the best wafer.

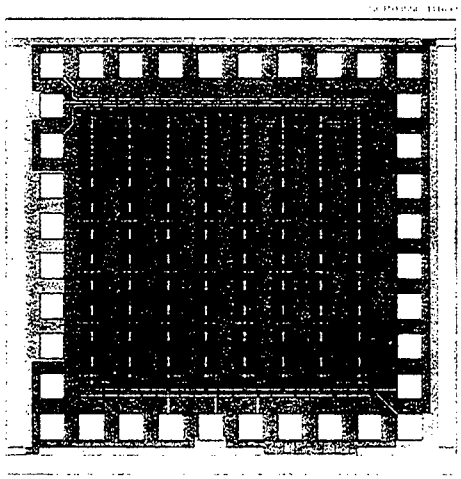


Figure 9. Microphotograph of a BiFET 32–bit × 2-bit shift register.

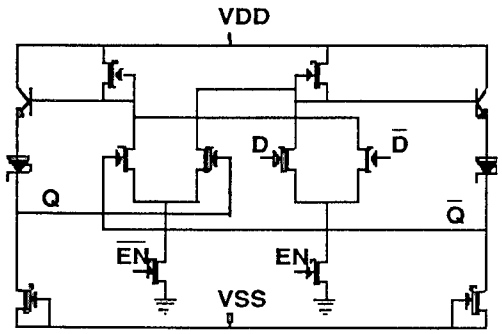


Figure 10. The basic buildingblock for a BiFET shift register.

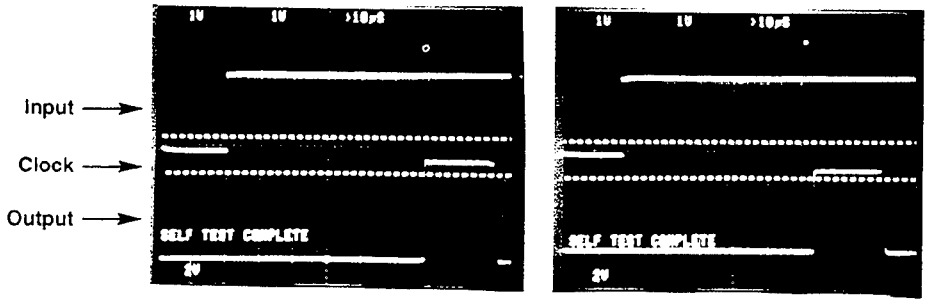
Sample and Hold Circuit

A BiFET sample and hold circuit (Figure 12) has been fabricated and evaluated. SINAD (Signal to Noise And Distortion) was measured to be greater than 55 dB, but was limited by our test setup. The device accepts differential analog input and produces differential output. Clocks at up to 200 MHz are differential, but were driven single-ended for this test. Twelve–bit performance (74 dB) was expected from the simulation; and nearly 9–bit performance was observed at 200 Msps with an input frequency of 198 MHz, despite our test setup limitations. The very low droop rates (10 Msps) offered by the BiFET technology were also verified. The photos (Figure 13) show the a signal with sampled output at 200 Msps and the spectrum of the beat frequency.

Ultrafast BiFET SRAM

A small size (64 bits) SRAM was fabricated and tested. It is a conventional design in which six address lines, a WR strobe, D_{in} and Q_{out} control all function. The Address lines are terminated with 50 ohms to ground; however, ECL levels may be used on all but the outputs. The outputs are complementary CML intended to be terminated with 50 ohms to ground. For testing purposes, all inputs are being run at CML levels.

The bit cell consists of four MESFETs and two HBTs (Figure 14). The two HBTs and two MESFETs form a cross-coupled latch, while two MESFETs are pass elements to complementary bit lines. The pass elements have gates connected to word lines. All peripheral circuitry is implemented in HBTs, with Schottky diodes used for row decoding.



Buffered HBT Logic (BHL) (a)

Buffered FET Logic (BFL) (b)

Figure 11. Functional BiFET 32 × 2–bit shift register with MUX on input: (a) Buffered HBT Logic (BHL), (b) Buffered FET Logic (BFL).

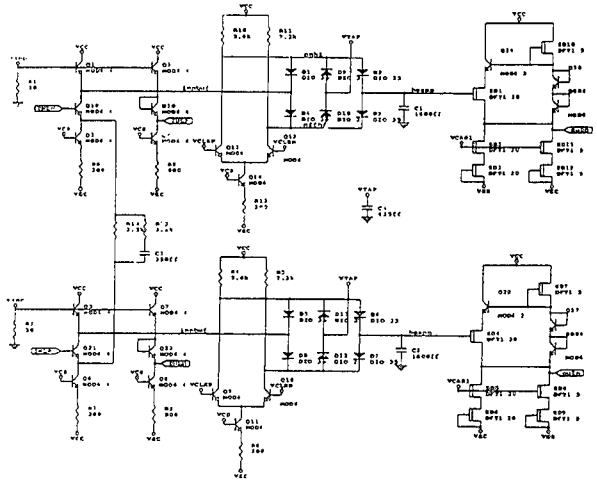
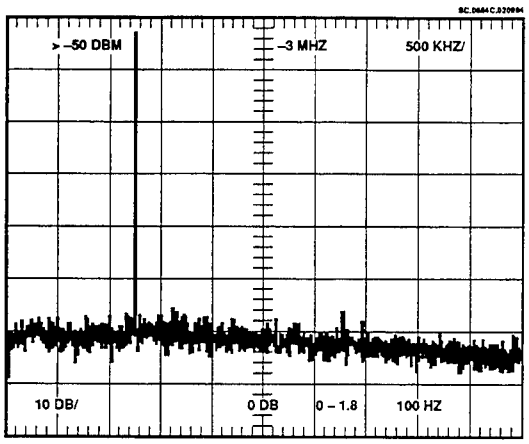


Figure 12. BiFET sample and hold circuit schematic.



Clock: 200 MHz
Input Signal Frequency: 198 MHz

Figure 13. BiFET sample/hold circuit output (SINAD > 55 dB).

An access time test was performed. The access time test consists of selecting an arbitrary address line (A5) and toggling it a 1 GHz. This is a column select and ought to represent a worst-case read access time. An HP54120 oscilloscope was used to capture the output and measure the delay. Access time of around 330 ps to 360 ps was observed (Figure 15). To our knowledge, this is the fastest SRAM ever demonstrated by any semiconductor technology.

Summary

In summary, we have developed a manufacturable, high performance GaAs BiFET technology for both analog and digital circuit applications. The technology is fully compatible with the standard HBT material growth and fabrication processes (only two additional masks needed to fabricate MESFETs and integrate them with HBTs). We have demonstrated the first BiFET LSI circuits including: a 2 Gsps 2-bit prototype DRFM, 2 GHz 32 × 2–bit word shift registers, sample and hold circuits with 9–bit resolution at 200 msps and SRAMs with very fast access time (330ps). The developed BiFET technology is anticipated to impact both military and commercial circuits and systems in areas of functionality, power, speed, noise and system architecture.

Acknowledgments

The authors gratefully acknowledge the support of AFWL (contract # F33615-90-C-1505) in pursuing this work.

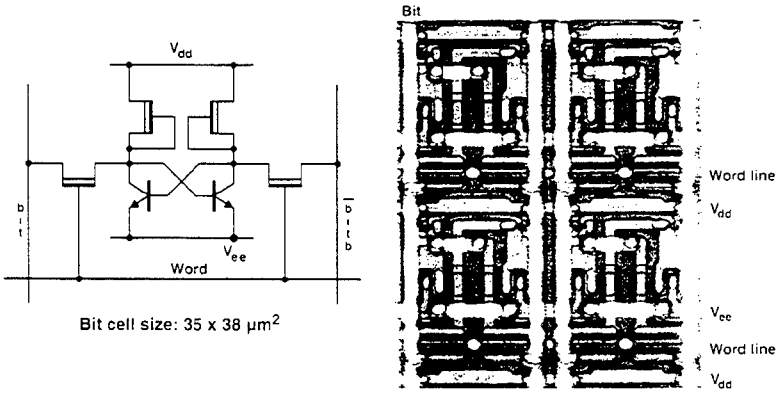


Figure 14. Schematic and microphotograph of BiFET memory cell.

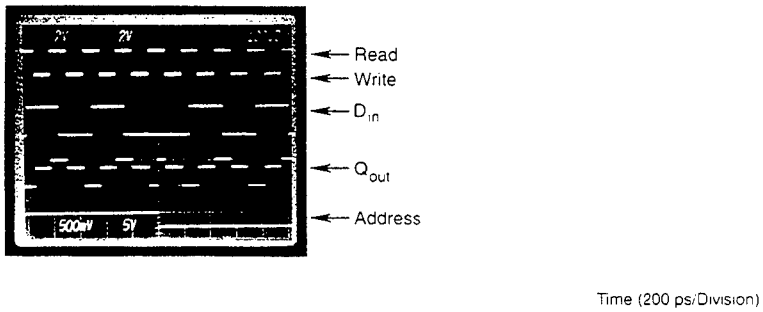


Figure 15. BiFET SRAM with read access time of 330 ps.

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GaAs on Insulator (GOI) for Low Power Applications

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The widespread use of wireless and mobile communication systems has necessitated the development of high frequency ultra-low power electronics. To minimize power consumption, it is essential to reduce the ungated electron currents in the on-state and the subthreshold leakage current in the off state. III-V semiconductors are attractive for low power applications because of high electron mobility and saturation velocity. This allows the reduction of the drain supply voltage without sacrificing the current drive, transconductance (g_m) and high frequency performance. However, the major drawback is the lack of an gate insulator (to allow for MOS technology) and a oxide buffer (to allow for equivalent of SOI technology). Recently, there has been an increased interest in the wet oxidation of AlAs, mainly for current confinement applications in optical devices [1,2]. We have developed insulated gate and oxide buffer technologies using the wet oxidation of AlGaAs to provide the insulator. In this paper the fabrication and performance of GaAs MISFET with Al_2O_3 gate insulator, GaAs on Insulator MESFET and pHEMT is presented. Also preliminary results using oxidized AlAsSb for the fabrication of oxide buffer AlInAs/GaInAs HEMTs is included.

GaAs MISFET with Al_2O_3 gate insulator

Low gate leakage in FETs is required for several applications, most notably low power high-speed ICs and high reliability power amplifiers. Furthermore, enhancement-mode FETs with low gate-leakage necessary for dense low power ICs are currently extremely difficult to achieve. An insulator gate would be a natural choice for high speed GaAs FETs with minimal gate leakage. However, GaAs based electronic devices still suffer from the lack of a suitable stable oxide.

A GaAs based FET with Al_2O_3 as the gate insulator was recently reported [3]. We have fabricated a GaAs MISFET with Al_2O_3 formed by the wet oxidation of AlAs as the gate oxide. Also the effect of hydrogenation in improving the device characteristics was studied [4].

Figure 1 shows the schematic diagram of a GaAs MISFET. The fabrication process is as follows. First, SiO_2 is deposited and patterned to open the source/drain regions (i.e the gate mesa is defined). Then we etch down to the channel using Cl_2 based RIE (wet etch is avoided to prevent any undesirable undercutting), thereby exposing the AlAs from the side. This is followed by the wet oxidation of AlAs. The steam oxidation is carried out in a single zone quartz furnace at 450°C, fed by a bubbler maintained at 85°C. The oxidation time is around 5 minutes which is sufficient to completely oxidize the AlAs layer under the gate laterally. The next step is Cl_2 based RIE etch to the buffer layer. After this, n+ GaAs is selectively regrown by MOCVD to form the source and drain contacts. The SiO_2 deposited initially, serves as the mask for the selective regrowth. Next, device isolation is accomplished by mesa etching, again. Tungsten is used to define the source, drain and gate electrodes. The use of a refractory metal (W) in conjunction with the MOCVD regrowth serves to form temperature stable contacts. Finally the devices were also subjected to a room temperature hydrogenation treatment with hydrogen ions at 400 eV for 30 minutes. The sample was tilted to enable the penetration of hydrogen to the gate oxide. The details of the hydrogenation system are described elsewhere [5].

The I-V characteristics of the MISFET before hydrogenation are shown in Figure 2. The FETs have a maximum drain current of about 50 mA/mm, and maximum transconductance g_m of about 7 mS/mm. The modulation of charge in the FET requires that the fermi level move freely through the gap and the presence of interface states can be readily observed via g_m compression at particular bias voltages in Figure 2. Figure 3 shows the I-V characteristics of the FET after hydrogenation. It is clear that the g_m compression is considerably reduced and the pinchoff

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characteristics have also improved. The g_m of the device after hydrogenation is enhanced and is around 15 mS/mm. This suggests that the interface state density at the oxide/GaAs interface is reduced by hydrogenation. We hypothesize that the interface states in this system arise mainly due to the excess Arsenic remaining after the oxidation of AlAs. This is supported by our DLTS study of the oxide formed by wet oxidation [6] which yielded a single dominant trap level at 0.74 eV, very close to the commonly observed As_{Ga} antisite. It has been shown that hydrogenation is helpful in removing the As as AsH_3 [5].

Forming a defect free oxide on GaAs is an extremely valuable pursuit. It will reduce leakage current in FETs at a minimum. Further reduction in the interface state densities to levels that would allow inversion will enable the fabrication of GaAs MOSFETs.

GaAs on Insulator (GOI) MESFETs and pHEMTs

There is no truly insulating buffer layer in III-V FET technology today. An insulating buffer gives excellent charge control which would make devices with high linearity and reduced dc-rf dispersion possible. It would also eliminate substrate leakage current, thereby improving output resistance of the FET. The GOI technology incorporates an insulating buffer layer in the conventional FET structure. The leakage current through the oxide insulator is in the $fA/\mu m^2$ range as determined from our previous MIS capacitor studies [6]. All the GOI technology requires in a regular FET epistructure is an additional $Al_xGa_{1-x}As$ layer which can be oxidized to form the insulator.

Figure 4 shows the epistructure for GOI MESFET. The processing is similar to that of a conventional FET except the process of oxidation of the AlAs buffer. Details of the fabrication process can be found in [7].

The DC characteristics and transfer of the GOI MESFET are shown in Figure 5 and 6 respectively . The current level is 300 mA/mm at a maximum g_m of 185 mS/mm. The g_m is high over a large range of gate voltage, implying good charge control and high linearity for the GOI MESFET. The equivalent circuit model is extracted from the S-parameter data. The channel resistance r_i is 1.3 Ω-mm and the f_t is 9 GHz and the f_{max} is 45 GHz. This is close to the intrinsic value for a 1.5 μm gate length GaAs MESFET (10.5 GHz assuming a velocity of 10^7 cm/s). The output resistance of the GOI MESFET is 320Ω-mm, giving the high f_{max}/f_t ratio. We have observed that the process of oxidation results in the reduction of current level due to the depletion of channel charge. To increase the current level, either the back depletion has to be reduced by lowering the state density at the oxide/semiconductor interface or the channel charge has to be increased to compensate for the depleted charge. The former is the desired long term solution because of its impact on improved 1/f noise and is being pursued.

The oxide buffer can also be incorporated into GaAs p-HEMTs which are now finding widespread used in wireless, microwave and millimeter wave circuits [8]. Figure 7 shows the epistructure of GaAs pHEMT. The fabrication process is similar to that of the GOI MESFET. The three-terminal DC I-V characteristics of the GOI p-HEMT as shown in Figure 8 (1.2 μm gate length device) indicate that the device has negligible output conductance. The peak g_m is 140 mS/mm at a drain current of 85 mA/mm as seen from Figure 9. The full channel current is around 140 mA/mm. The pinch-off characteristics are excellent, implying good charge control in the GOI p-HEMT. The decrease in current level after oxidation is more that in the case of GOI MESFET due to aggressive oxidation conditions, optimization of the oxidation process is currently under progress.The f_t and f_{max} of this device are 6.4 GHz and 16 GHz respectively. These are lower than those expected for a 1.2 μm gate length device due to the low current level in the device which increases the series channel resistance.

AlInAs/GaInAs HEMT on oxide buffer

AlInAs/GaInAs based HEMTs have lower power consumption and better high frequency performance than GaAs based HEMTs due to higher electron mobility and sheet charge density. Oxide based electronics holds great promise in the AlInAs/GaInAs/InP material system for ultra-low power high frequency applications. Gate insulators and oxides buffers can be formed in the

InP based material system by using oxidized AlAsSb. Steam Oxidation of AlAsSb lattice matched to InP at 350 °C has been reported previously [9]. The differentiating aspect in this case from AlGaAs is the formation of a semimetallic Sb layer at the top of the oxide. This is undesirable as it prevents the oxide from being used as a insulating buffer. However we have observed that oxidation at higher temperatures (450 °C) reduces the amount of Sb in the oxide. This oxidation temperature is still low enough to prevent the oxidation of the AlInAs layers.

Figure 10 shows the epistructure for AlInAs/GaInAs HEMT with oxide buffer. It consists of a standard AlInAs/GaInAs HEMT structure with the exception of a 500 Å AlAsSb buffer and a n+InGaAs/n+ AlInAs doped cap for non-alloyed contact. The fabrication process is similar to that of GOI MESFETs and pHEMTs. The AlAsSb oxidation is carried out at 450 °C for 30 minutes with nitrogen bubbling through water kept at 90 °C [10].

Figures 11 and 12 show the three terminal I-V characteristics and the transfer characteristics of the oxidized AlAsSb buffer HEMT. The drain current is 55 mA/mm and the transconductance is 176 mS/mm at Vds=1.5 V, Vgs=0.0 V. The output conductance is 13 mS/mm. This technology enables the formation of an insulating buffers and interlayer dielectrics for the AlInAs/GaInAs/InP material system and has applications in low power complementary HFET technology.

To summarize oxide based electronics in the GaAs and InP based material systems shows great promise for ultra-low power high frequency applications. A detailed characterization of the oxidation process and its effect on the material and electrical properties of FET epistructures is necessary to fully exploit the advantages offered by insulating dielectrics and buffers in the III-V FET technology.

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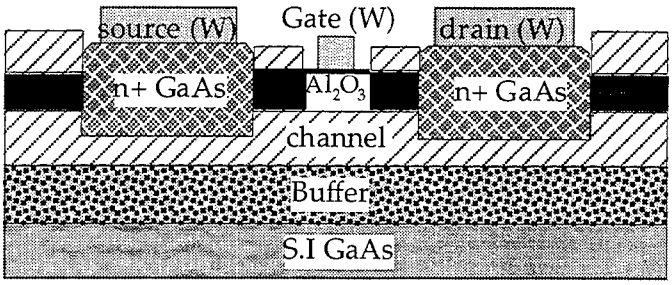

Fig.1 Schematic diagram of GaAs MISFET

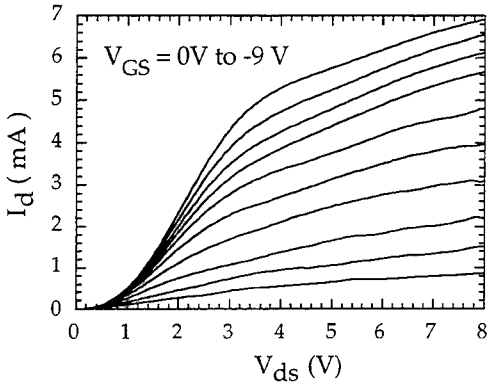

Fig.2 : I-V Characteristics of GaAs MISFET before hydrogenation

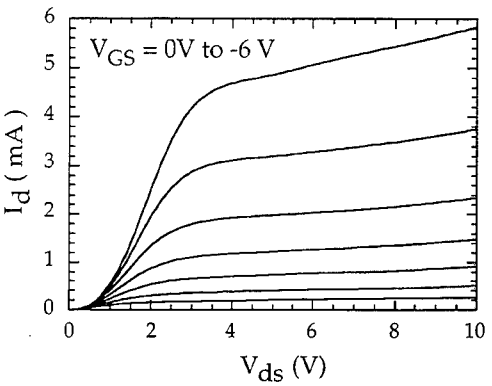

Fig.3 I-V Characteristics of GaAs MISFET after hydrogenation

n+ grade to InAs
30 Å $Al_{0.7}GaAs$ etch stop
1000 Å GaAs channel $3x10^{17}/cm^3$
100 Å $Al_{0.3}GaAs$ spacer
500 Å AlAs
2000 Å Buffer
S.I GaAs

Fig. 4 : Epi-structure for GaAs on Insulator (GOI) MESFET

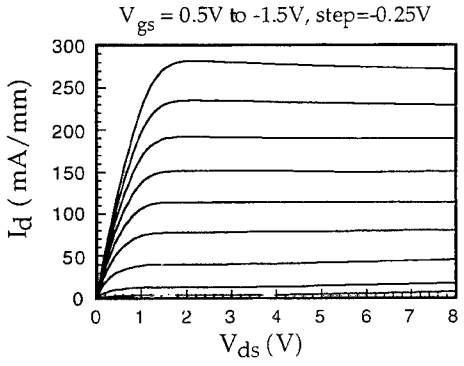

Fig.5 : I-V Characteristics of GOI MESFET

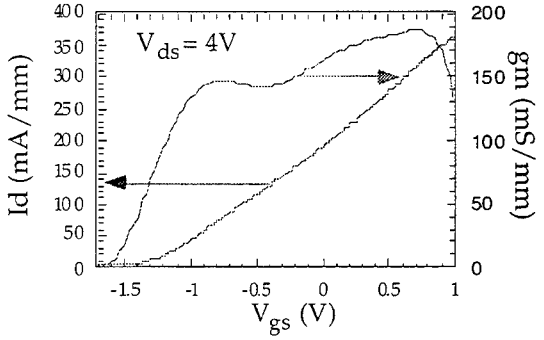

Fig. 6 : Transfer Characteristics of GOI MESFET

200 Å InAs/GaAs n+ ohmic cap
30 Å $Al_{0.7}GaAs$ etch stop
250 Å $Al_{0.25}GaAs$ barrier
δ - doping $5x10^{12}/cm^2$
30 Å $Al_{0.25}GaAs$ spacer
75 Å $In_{0.2}GaAs$ channel
δ - doping $1x10^{12}/cm^2$
75 Å $In_{0.2}GaAs$ channel
50 Å $Al_{0.25}GaAs$ spacer
δ - doping $2x10^{12}/cm^2$
100 A $Al_{0.25}GaAs$ spacer
500 A $Al_{0.98}GaAs$ oxidation layer
3000 Å GaAs buffer
S. I. GaAs Substrate

Fig. 7 : Epistructure for GOI pHEMT

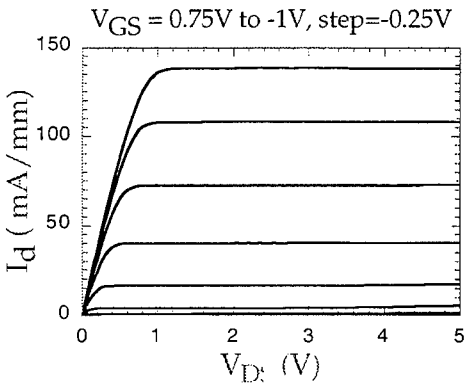

Fig. 8 I-V Characteristic for the GOI p-HEMT

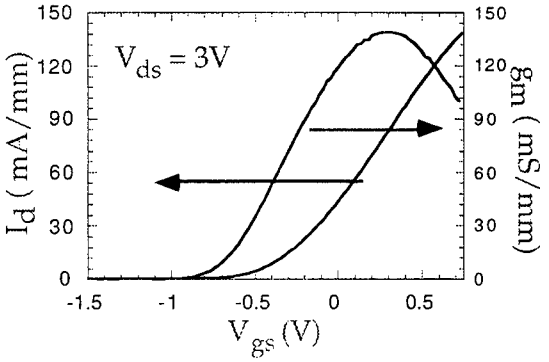

Fig. 9 Transfer Characteristics for the GOI p-HEMT

150 Å n+ GaInAs $n=1.2x10^{19}$ cap
150 Å n+ AlInAs $n=1.2x10^{19}$ cap
175 Å i-AlInAs barrier
40 Å n+ AlInAs $n=1.2x10^{19}$donor layer
30 Å i-AlInAs spacer
400 Å i-InGaAs channel
100 Å i-AlInAs spacer
500 Å AlAsSb buffer
200 Å i-AlInAs buffer
S.I. InP substrate

Fig. 10 : Epistructure for AlInAs/GaInAs HEMT on Oxide Buffer

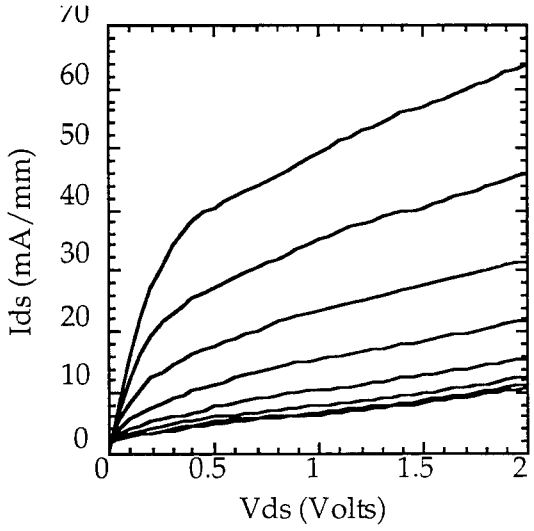

Fig.11 : I-V Characteristics of HEMT with oxidized AlAsSb buffer

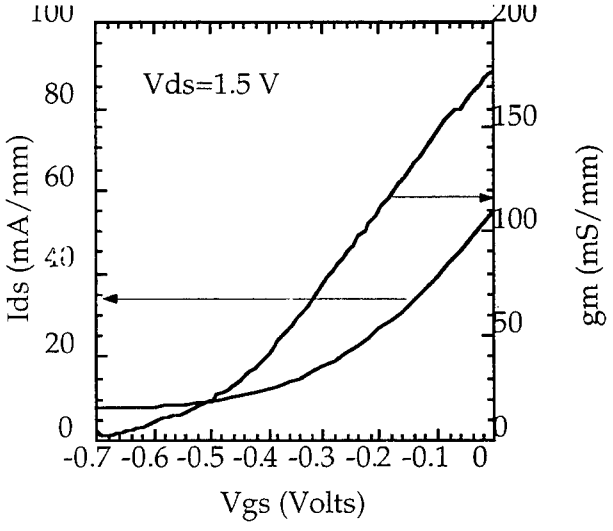

Fig.12 Transfer Characteristics of HEMT with with oxidized AlAsSb buffer

Epitaxy-on-Electronics Enhancement of GaAs IC Performance with Monolithic Optical and Quantum-Effect Devices*

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Abstract

An integration technique, Epitaxy-on-Electronics (EoE), is described wherein optoelectronic and quantum effect device heterostructures are grown on fully processed GaAs integrated circuit chips and subsequently processed into devices monolithically integrated with the pre-existing circuitry. Using this technique, one can realize the increased performance and functionality promised by adding advanced heterostructure quantum effect and optoelectronic devices to conventional integrated electronic circuitry, without developing a complete new VLSI technology. The details of the EoE technology are explained, and examples of optoelectronic integrated circuits incorporating LEDs, detectors, and MESFET electronics are presented. The OPTOCHIP Project, a prototype EoE research OEIC foundry, and work on EoE integration of resonant tunneling diodes to form one-transistor GaAs static random access memory cells, are also described.

Introduction

Enhancing the functionality of conventional electronic circuits with optical and quantum-effect devices has long been recognized as a desirable, though challenging, goal. The implementation of advanced optical interconnect architectures, for example, require optoelectronic integrated circuits (OEICs) consisting of thousands of optoelectronic devices closely coupled with VLSI-complexity electronics. Hybriding, wafer-bonding, and epitaxial lift-off have made progress addressing this need, however issues of density, performance, manufacturability, and reliability make a monolithic integration technique preferable. Monolithic integration on silicon VLSI has been hampered by the difficulty of III-V growth on Si, and monolithic integration on III-V substrates has been limited to small scale integration when the electronic and optoelectronic technologies must both be developed.

The success of commercial GaAs VLSI technology offers another solution: true VLSI-complexity heterostructure-enhanced integrated circuits without the barrier of substrate-mismatched growth. The technique invented at MIT known as Epitaxy-on-Electronics (EoE) uses a commercially processed GaAs IC as the starting point for the growth and fabrication of integrated optoelectronic and/or quantum effect devices. In the following sections, the EoE technique will first be described and explained, and recent results and current research on the application of this technology to realizing complex optoelectronic integrated circuits and to enhancing electronic circuits with quantum-effect devices are summarized.

Epitaxy-on-Electronics Technology

One of the basic tenets of the EoE approach is that one enjoys significant advantage by building upon an existing VLSI technology base, rather than attempting to develop simultaneously the technology to make both VLSI-level electronics and optoelectronic

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(and/or quantum-effect) devices. Thus in EoE the integrated circuit technology is taken as a "given" and without modification from the manufacturer of choice [1]; the heterostructure devices are added to commercially-processed, state-of-the-art, custom integrated circuit wafers (or, in the present development phase, chips obtained through a foundry service [2]) after the manufacturer has completed its processing.

The upper surfaces of commercially-processed integrated circuits are covered with alternating layers of metal interconnect patterns and dielectric insulation totaling 5 to 10 microns thick. In the EoE process vias are cut through this dielectric stack down to the original substrate surface wherever heterostructure devices are to be subsequently integrated. These vias, termed dielectric growth windows (DGWs), are specified during the circuit layout process, and they are created by the IC manufacturer in the course of normal processing. We have recently introduced a new DGW design which has proven much easier to clean fully without damaging the underlying substrate than previous designs.

After the custom circuits are received from the manufacturer, the DGWs are cleaned further and the required heterostructure is grown, as illustrated in Figure 1. Single crystal layers grow in the DGWs, and polycrystalline material deposits elsewhere; the structure is designed so that the upper surface of the crystalline heterostructures in the DGWs is level with the upper surface of the dielectric stack. The polycrystalline deposit is subsequently removed and the heterostructures are processed using standard techniques into devices monolithically interconnected with the pre-existing electronics (see Fig. 1c). Electrical contact is made via metal lines patterned between ohmic contacts on the devices to contact pads included on the IC, and/or through a doped region patterned under the DGW.

The GaAs IC process uses aluminum-based interconnects common in silicon technology. As such, the interconnects are degraded if exposed to excessive temperatures [3]. This requires that the typically five-to-six-hour heterostructure growth cycle be carried out below 475°C, which is a relatively low growth temperature for many epitaxy techniques and materials, and special steps have to be taken to deal with it. For example, traditional molecular beam epitaxy (MBE) grown AlGaAs-based emitters do not function well when grown below 600°C, a fact which limited the performance of early EoE OEIC demonstrations [4]. Aluminum-free, phosphide-based heterostructures which are much more compatible with reduced-temperature growth (by gas source MBE) are now used extensively for emitters, while aluminum-containing layers are restricted to modulators, detectors, majority-carrier quantum-effect devices, and some passive regions in emitters.

475°C is also much lower than the temperature normally used to desorb any surface oxide prior to MBE. Only a few seconds above 580°C is required, but even this results in some degradation in circuit performance. To overcome this problem, atomic hydrogen removal of the oxide has recently been introduced. This process can be done with the substrate temperature under 400°C, and no degradation in circuit performance is seen.

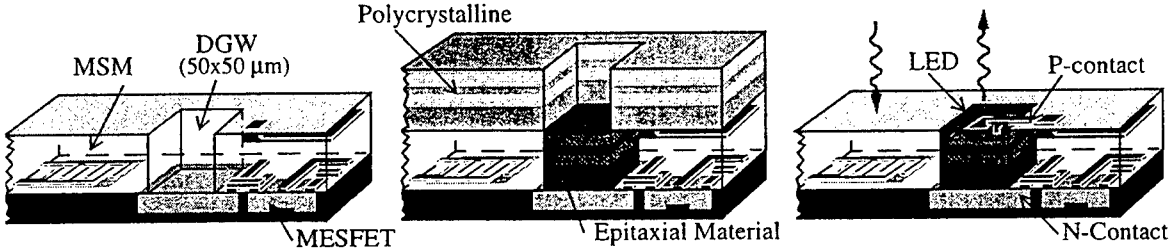

Figure 1: The Epitaxy-on-Electronics process: A region on a chip containing a DGW (a) prior to epitaxy; (b) after epitaxial growth, and (c) after removal of the poly-crystalline deposit and completion of device processing and interconnection.

OEICs and the OPTOCHIP Project

The first target application of the EoE process was in optoelectronic integration. The initial driving force was surface-normal, "smart pixel array" type applications in which there is typically significant electrical communication between pixels in a given array, and massively parallel optical communication at 860 nm between smart pixel arrays. Other applications now also being pursued are surface-normal receivers and transmitters at 1550 nm for fiber communications, and in-plane "integrated-optics" type geometries, also for fiber applications. At 860 nm, photodetectors (specifically m-s-m detectors and optically-sensitive FETs called OPFETs) can be fabricated as part of the IC process. The challenge then becomes fabrication efficient emitters by the EoE process. To be compatible with the MESFET electronics, these emitters should operate from a 2.2 V supply and the total device heterostructure must be less than 6 μm thick.

The easiest device to integrate is a light emitting diode (LED), and this was done first in the AlGaAs system [4], and more recently using aluminum-free phosphides [5]. The latter devices are several orders of magnitude more efficient, with external quantum efficiencies approaching 1.2%, and with output powers in excess of 30 μW at a drive voltage under 2 V. A representative completed EoE OEIC with an LED in operation is illustrated in Figure 2.

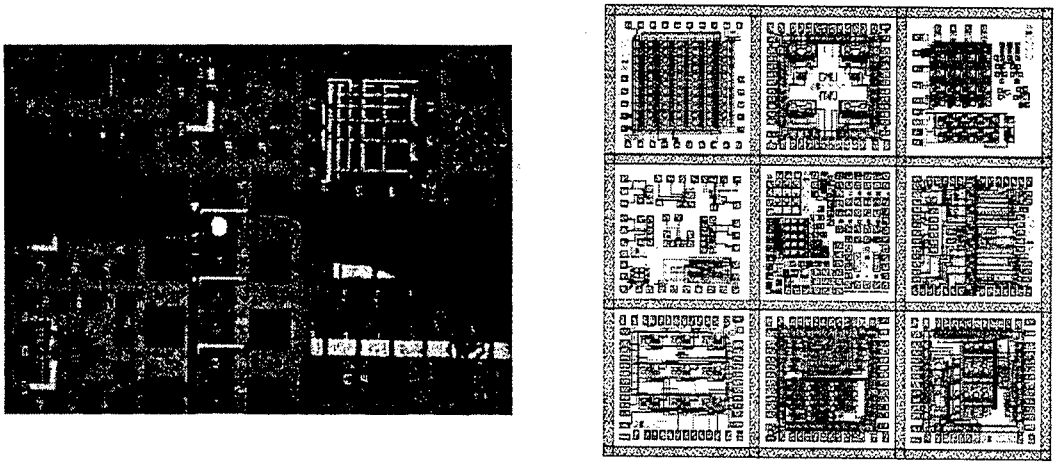

Figure 2: LEFT: A completed EoE optoelectronic integrated circuit with one of the integrated light emitting diodes in operation. The central emitting area of the LED is 11.5 μm by 16 μm, and the DGW in which it was grown is 50 μm square. RIGHT: The layout of the OPTOCHIP, a 7 mm square EoE OEIC chip combining designs from 9 research groups from the US and Canada, currently being processed at MIT.

In-plane lasers have been fabricated in aluminum-free InGaP/InGaAs heterostructures grown at 470°C on GaAs substrates which have broad-area thresholds of 220 A/cm^2. Work is now in progress on integrating surface emitting lasers by the EoE process. Both in-plane surface-emitting lasers (IPSELs) and vertical-cavity surface-emitting lasers (VCSELs) are being developed.

While lasers are most desirable emitter for most OEIC applications, there is still a great deal of interest in integrated LEDs and much that can be done with them. Consequently, a research foundry service, the OPTOCHIP Project, was offered to researchers in late 1995 and eighteen groups submitted proposals to participate. Nine groups were selected and each submitted a design for a 2 by 2 mm OEIC chip containing enhancement and depletion mode MESFETs, msm and OPFET detectors, and 50 μm square DGWs for LEDs; there were no limits on device counts, and a wide variety of designs was submitted in May 1996 [5]. The designs were combined into a single chip layout, illustrated in Figure 2, submitted to MOSIS

[2] and received in August. When EoE processing is completed, the chips will be divided into individual project chips and distributed to the participating groups in early 1997.

Quantum Effect Device Enhancement

Quantum effect devices, most notably resonant tunneling diodes (RTDs), have been proposed as high functionality complements to conventional digital circuits, and careful consideration indicates that one of the most immediate needs for such enhancement is in the area of III-V memories. Dynamic memories are difficult to realize because of high Schottky barrier leakage, and thus static memories requiring six or more transistors per cell must be used. A very attractive alternative is a single-transistor, two-RTD SRAM cell proposed by several groups [6]. The viability of using the EoE process to integrate RTDs on GaAs MESFET chips to produce such SRAM cells has been demonstrated by R. J. Aggarwal at MIT [6]. The challenge of producing high peak-to-valley current ratio RTDs on GaAs was also addressed in this work [7]. Future work needs to focus on the issue of minimizing the size of the DGWs, and maximizing the packing density of EoE RTD SRAM cells.

Conclusion

With the recent introduction of three key processing innovations (i.e., a new DGW design, aluminum-free phosphides, and atomic hydrogen oxide removal) the EoE process has been developed to the point that it can easily be adopted and employed by other groups for applications requiring the integration of large numbers of optoelectronic and quantum-effect devices with high-performance, VLSI-density and -complexity FET electronics. Curernt work at MIT focuses on further refining the process, and, in particular, on increasing the menu of devices available in EoE to include laser diodes (860 nm), longer wavelength (1550 nm) detectors and emitters, integrated optics components, and modulators. Work is also in progress evaluating the Vitesse HGaAs-4 process for EoE applications; this technology is well suited for analog, as well as digital, applications, and offers still higher speed circuitry.

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1. The GaAs integrated circuits used in this work contain enhancement- and depletion-mode MESFETs, and are manufactured by Vitesse Semiconductor Corporation, 741 Calle Plano, Camarillo, CA 93010, using their HGaAs-3 process.

2. The Vitesse HGaAs-3 process is available to users of the MOSIS service operated for NSF and DARPA by the University of Southern California Information Sciences Institute, 4676 Admiralty Way, Marina del Rey, CA 90292-6695.

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5. Additional information on the OPTOCHIP Project can be found on the World-Wide Web at

6. A good overview of these issues, and of EoE research in this area, can be found in the PhD thesis of R. J. Aggarwal: "Design of Resonant-Tunneling Diodes for a GaAs Integrated SRAM," Department of Electrical Engineering and Computer Science, M.I.T., Cambridge, MA, Feb. 1996.

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Application of High ε Paramagnetic and Ferroelectric Materials to High-Transconductance HFETs with Low Noise and Low Gate Current

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1. Introduction

The main problem in high-transconductance FET's is the presence of a considerable gate leakage current that loads the input and reduces the power amplification coefficient. The problem has become particularly serious in InGaAs Heterostructure FET's.

Indeed, to achieve a high transconductance, the gate capacitance must be high, and the gate insulation must be thin. This leads to tunneling currents through the gate insulation.

A detailed examination of the quantum-mechanical tunneling problem by these authors in cooperation with F. Schuermeyer in 1993-1996 shows that the only way to reduce the gate tunneling current without sacrificing the gate capacitance is to use materials with high dielectric constant ε_r as insulators under the gate.

It is obvious that only amorphous ferroelectric materials with negligible remanent polarization and high coercive field are useful if we want to avoid the hysteresis effect, and are interested only in suppression of the leakage currents in high transconductance devices. For certain applications, hysteresis in the response of the device is desirable, and should be achievable by slight modifications in the fabrication process. The present paper analyzes the possibility of using ferroelectric and paraelectric high ε gate insulators, including also noise considerations, in particular quantum 1/f noise.

2. General Considerations

An increased gate capacitance is particularly desirable at lower frequencies, because it leads to higher transconductances of the FET, without compromising its desirable large input impedance. At high and ultrahigh frequencies, however, a very large gate capacitance C is less desirable, because it essentially shorts the gate to the channel and requires large capacitive gate currents and signal power input levels at the achievable f_τ and f_{max} values. The natural solution that allows for a smaller frequency dependence of the input admittance $j\omega C$ is a ferroelectric gate insulation. Indeed, at low frequencies, it could increase the gate capacitance and device transconductance by a factor of 10^2, while at higher frequencies, where such a large capacitance could be harmful, the dielectric constant decreases to intermediate values, allowing for operation at the highest frequencies with a reasonable input impedance. This is the main advantage of a ferroelectric gate insulation.

Unfortunately, the ferroelectric introduces its own resonances and their characteristic frequencies, as well as dissipation. Furthermore, if leakage through

the ferroelectric is still occurring, it leads to a normalized quantum 1/f noise coefficient larger by a factor of 10^6 than what we would get without piezoelectric coupling of the current carriers.

A possible way for reducing the remaining frequency dependence of the gate capacitance is the use of two or more ferroelectric layers. This introduces additional resonances and resonances corresponding to the space-charge relaxation at the interfaces. However, in return, each of these resonances could be weighted down so that the resulting frequency dependence will just present small nonuniformities which cause negligible spectral distortion in amplifiers.

3. History

The effect of ferroelectric polarization on insulated-gate thin film transistor parameters was first studied by Zuleeg and Wieder[1] as a device for non-volatile memory design. They applied a 1 mm thick film of ferroelectric TGS (tri-glicine-sulphate) on one side of a 5,000Å CdS film as gate insulation, the other side of the film being insulated by 1000Å of SiO_2 from an Al gate. Gold was used for the gate applied to the TGS, the source and the drain contacts. Depending on the polarization state of the TGS, controlled by the gold gate voltage, and by its previous voltage history, one gets various sets of drain characteristics. In the metal-ferroelectric semiconductor structure, proposed later by Wu [2], a thin film of ferroelectric $Bi_4Ti_3O_{12}$ was replacing the oxide of a MOSFET. This was suggested as a new ferroelectric memory device. The materials PZT, i.e., $PbZr_xTi_{1-x}O_3$ [3] and $LiNbO_3$ [4] were investigated as ferroelectric gate insulators, as well as other materials [5]. However, all these materials contain oxygen, and will cause oxidation of the compound semiconductors.

On the other hand, the nature of the leakage current was investigated in HFETS by Schuermeyer et. al., [6]-[7]. They focused primarily on the thermal activation of carriers from the channel over the barrier separating them from the gate. These authors found that the density of the thermal activation current reached a maximum at an intermediary region, closer to the drain than to the source. In the present paper, we illustrate the application of ferroelectric or high ε materials to the case of the InGaAs/AlGaAs/GaAs and InGaAs/InAlAs/InP enhancement-mode HFETs fabricated and studied by Schuermeyer et. al., [6]-[7].

4. Approach

We will consider the ferroelectric material $BaMgF_4$ as a leading candidate for coating the barrier layer, applying it in its amorphous form at 450° C on the external AlGaAs barrier layer, separating the channel from the gate of the HFET. In this form it has negligible hysteresis and is characterized by a dielectric constant ε_i=35. The deposition temperature is not too high for the HFET. The AlGaAs barrier thickness d can be reduced to 15 nm and the $BaMgF_4$ layer needs to be only 20 nm thick. Fig. 1 and 2 show the approximate device structure and the conduction band configuration for an n-channel HFET.

To further clarify our approach, we use the simple FET expression for the intrinsic transconductance g_m

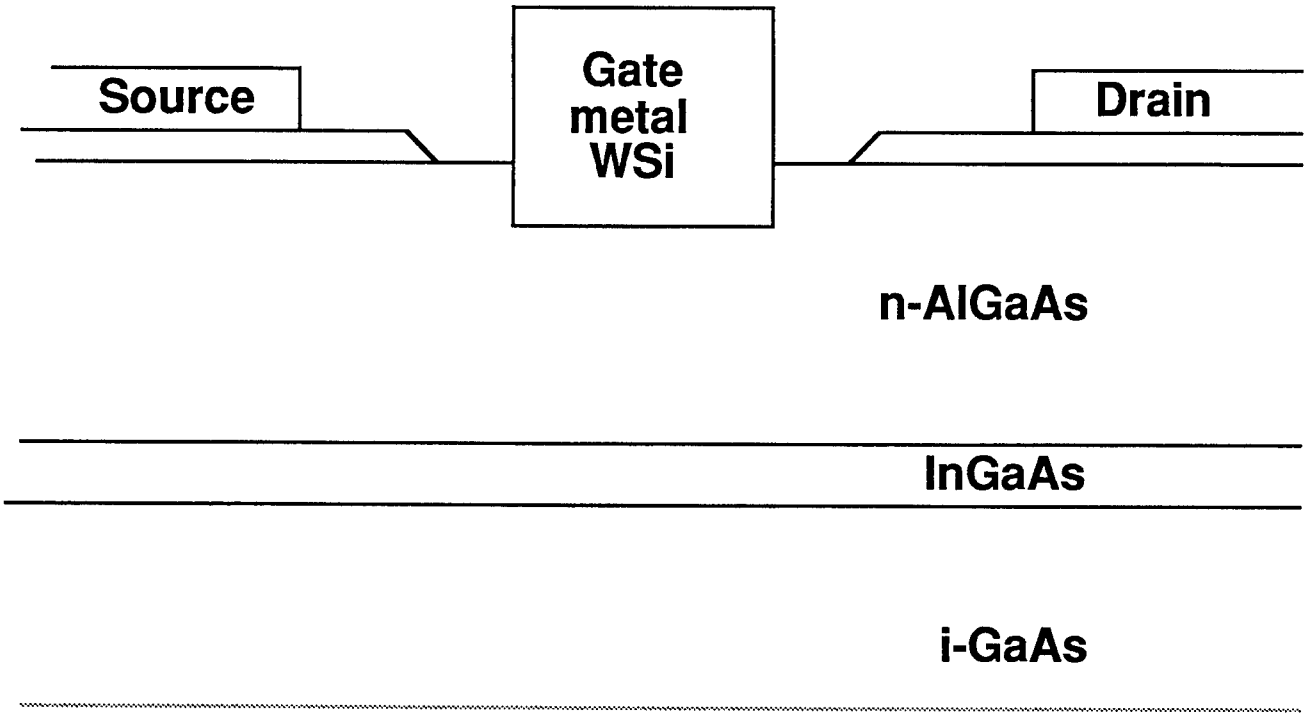

Fig. 1: HFET structure.

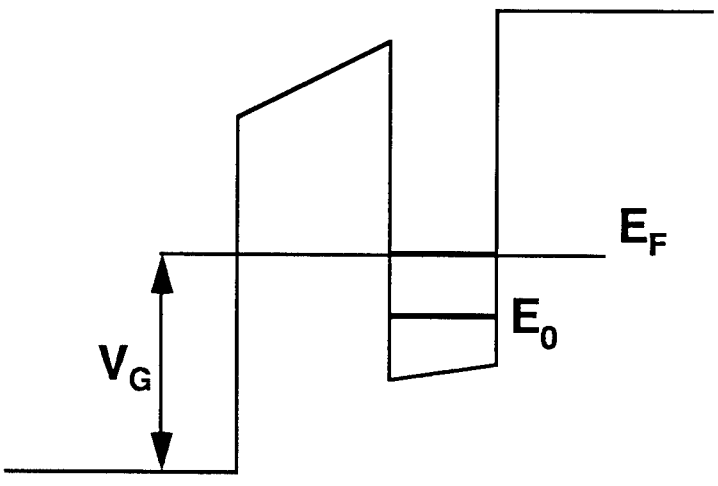

Fig. 2: HFET Band Structure

$$g_m = \frac{C_G}{t_c}, \quad \text{with } C_G = \frac{\varepsilon LW}{t_{ins}} \tag{1}$$

$$\text{and } t_c = \frac{L^2}{2\mu V_D} \text{ for low field, or } t_c = \frac{L}{v_m} \text{ for high field.} \tag{2}$$

Here C_G is the gate capacitance, t_c the effective channel transit time, ε the effective permittivity of the gate capacitance, L the gate length, W its width, t_{ins} the effective distance between gate and channel, equivalent with a total insulation thickness, μ the effective channel mobility, V_D the source-drain voltage, and v_m the maximal drift velocity obtained in the high field regime of the channel.

From Eqs. (1) and (2) we see that by increasing t_{ins} by a factor λ and ε by a factor λ^4, g_m will increase by a factor of λ^3. At the same time the leakage current caused by tunneling through the barrier will become negligible for all practical purposes for $\lambda \geq 2$, because the tunneling probability $T \ll 1$ will be replaced by $\leq T^2$. Indeed, an additional decrease of the gate current will be caused by the reduction of the electric field present throughout the barrier.

The unit current gain frequency, f_τ, is not affected, being approximated by

$$f_\tau = 1/2\pi t_c. \tag{3}$$

However, the maximum frequency of oscillation, f_{max}, is given by

$$f_{max} = (f_\tau/2)(g_m/g_{out})^{1/2}, \tag{4}$$

where g_{out} is the output conductance that is not affected by C_G or by λ. The maximum frequency of oscillation is therefore increased by $\lambda^{3/2}$, provided there is no decrease in ε at $f=f_{max}$. For instance, with $\lambda=1.41$, increasing t_{ins} 1.41 times and ε 4 times will increase g_m 2.82 times, f_{max} 1.65 times and stop the gate current. Actually, there will be a considerable decrease of ε at high frequencies, and therefore, we expect f_{max} to increase less than predicted by the factor $\lambda^{3/2}$.

5. $BaMgF_4$ Technology

The ferroelectricity of $BaMgF_4$ was discovered in 1969. However, this material was not fabricated as a thin film till 1989, and was first deposited on Si surfaces to generate ferroelectric memory FETs [8]. It has been found that $BaMgF_4$ grown on GaAs or AlGaAs (100) surfaces at 450°C is amorphous [9]. As seen [9] in Fig. 3, this film does not exhibit hysteresis, but is a paraelectric insulator with a relative dielectric constant ε_r of 35. Fig. 3 shows the polarization P in $\mu C/cm^2$ as a function of the applied field in kV/cm. The substrate was (100) n-type GaAs at 450°C. The growth rate was 0.4 μm/h.

At temperatures of 500-600°C polycrystalline ferroelectric films exhibiting hysteresis were grown, with a (140) orientation. Their coercive field was about 200kV/cm and the remanent polarization P_r about 1.3 $\mu C/cm^2$. For monocrystalline material the expected value of P_r is 4 $\mu C/cm^2$.

In order to obtain high-g_m HFETs with truly negligible gate currents, we therefore recommend choosing the factor λ defined in Sec. 4 to be $\sqrt{2}$. We thus

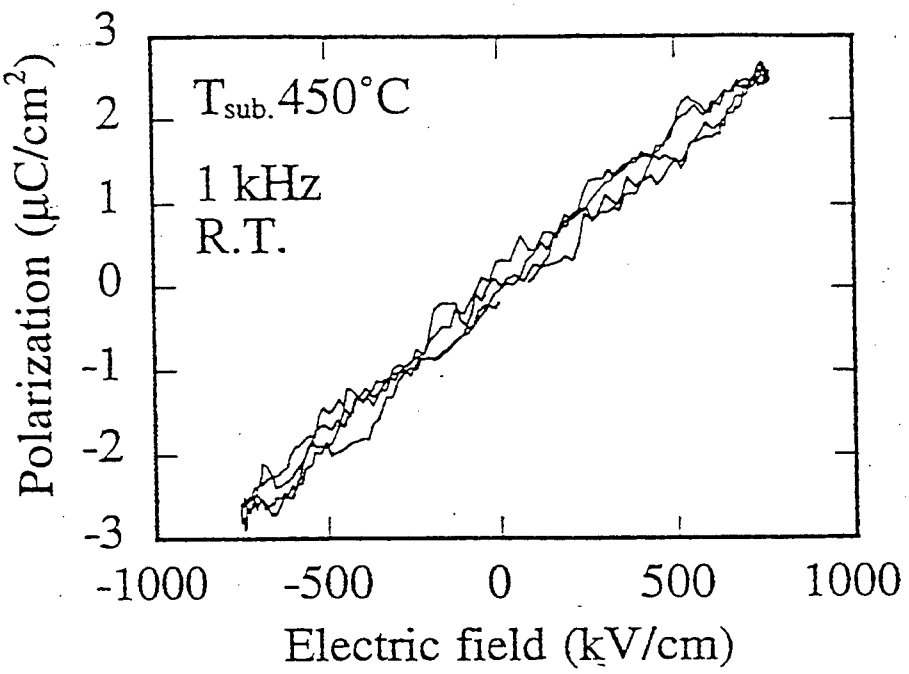

Fig. 3. Typical *P-E* hysteresis plot of the amorphous $BaMgF_4$ film grown on the n-type GaAs(100) substrate at 450°C.

obtain a transconductance increased by a factor of $2\sqrt{2}$, a total barrier thickness increased by a factor of $\sqrt{2}$, and therefore a negligible gate current. Practically, this is achieved by properly structuring the barrier grown on the undoped GaAs channel. First a 5 nm undoped AlGaAs spacer layer is deposited on the channel, then 10 nm of n-type AlGaAs, followed by 20 nm of amorphous $BaMgF_4$, and by the metal of the gate electrode, e.g., Al.

By varying the growing temperature and speed in the interval of 450-495°C and around 0.4 μm/h, we may be able to achieve a useful further increase in ε without detrimental hysteresis effects.

6. 1/f Noise

The 1/f noise of the 2-DEGrees-of-freedom-electrons in the conducting InGaAs channel is determined by the conventional quantum 1/f formula for polar optical scattering at 300K, or for the mixture of polar optical phonon, longitudinal acoustical phonon, piezoelectric, and lattice defect scattering at 70K. The spectral density S of fractional quantum 1/f fluctuations $\delta\Gamma/\Gamma$ of the electron scattering rate Γ in a process with velocity change Δv of the electrons is

$$S_{\delta\Gamma/\Gamma}(f) = 2\alpha A/fN = (4\alpha/3\pi fN)(\Delta v/c)^2. \quad (5)$$

Here $\alpha=e^2/\hbar c=1/137$ is the fine structure constant, $A=(2/3\pi)(\Delta v/c)^2$, c is the speed of light and N is the number of electrons used in defining the rate Γ. The fractional quantum 1/f fluctuation $\delta\Gamma/\Gamma$ of the electron scattering rate Γ on a polar optical phonon of momentum $\hbar q$ and energy $\hbar\omega_q \approx \omega_0$ is given by the spectral density

$$S_{\delta\Gamma/\Gamma}(f) = (4\alpha/3\pi fN)\langle(\hbar q/m^*c)^2\rangle = (4\alpha/3\pi fN)(2\hbar k/m^*c)^2. \quad (6)$$

Here we have estimated the average quadratic momentum change of the electrons, resulting from the momentum $\hbar q$ of the optical phonon to be $2(\hbar k)^2$, because the momentum transfer to electrons of momentum $\hbar k$ is known [7] to be between the limits $\hbar q_{min} = \hbar\{-k+[k^2 + 2m^*\omega_o/\hbar]^{1/2}\}$ and $\hbar q_{max} = \hbar\{k+[k^2 + 2m^*\omega_o/\hbar]^{1/2}\}$. Eq. (6) yields a spectral density

$$S_{\delta\Gamma/\Gamma}(f) = 10^{-7}/fN = S_{\delta\mu/\mu}(f) = S_{\delta I/I}(f) \quad (7)$$

where I is the source to drain current, and N the number of carriers in the channel. The expected rms drain current fluctuation amplitude is thus $3.16\,10^{-4}\, I_d/N\sqrt{f}$. Both through N and through the drain current I_d this simple result depends on the applied gate voltage V_G.

7. Conclusions

The preceding discussion indicates that a paraelectric or hysteresis-free ferroelectric gate insulation is ideal for special HFETs meeting bandwidth requirements from 0 to 100 GHz. It allows total suppression of gate leakage currents, while also assuring a large increase in the transconductance of the device at frequencies under 100 MHz, where the permittivity is still high.

The gradual decrease of ε in the UHF region is actually very useful, since it limits the free fall of the input impedance $(j\omega C)^{-1}$ of the device to zero, which would load the source excessively.

Finally, the lower temperature $BaMgF_4$ technology avoids oxidation and degradation of the compound semiconductors, and a further improvement in ε through mobile ferroelectric micro-domains is possible by optimizing the growing conditions.

The authors are indebted to F. Schuermeyer for suggesting the research for elimination of gate currents and for many helpful discussions. They acknowledge the support of AFOSR and NSF.

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Optoelectronics

Hot electrons in quantum cascade lasers

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Abstract. We have developed a theory describing the operation of lasers based on intersubband transitions in a quantum well. The theory combines a first-principles description of the intersubband lineshape and the optical gain with kinetic models for carrier heating. The theory is consistent with the experimental data available and suggests new ways of improving the laser design for room temperature operation with high output power. At low carrier concentrations, it is possible to achieve positive values of the gain at room temperature even in the absence of an overall population inversion between quantum well subbands. For higher (but still moderate) concentrations, the theory predicts a peculiar dependence of the output wavelength on the pump current, including a regime where the lasing wavelength switches "digitally" between two stable values.

The quantum cascade laser is a new mid-infrared laser, based on unipolar transitions of electrons between energy levels created by quantum confinement. Since the first demonstration of QCL (Faist et al. 1994), its design has continuously improved through a series of elegant innovations by the Bell Labs group (Faist et al. 1995a,b) culminating in their recent report of a high power room-temperature operation (Faist et al. 1996).

The device has multiple periods (25 in reported structures) and each electron performs a cascade of transitions down the periodic ladder. Under the operating conditions, each period must have net zero charge: by Gauss' law this is necessary in order that subsequent periods could replicate each others electrostatic state. To avoid the space charge accumulation, associated with current flow, one therefore needs a reservoir of positive fixed charge, compensating the negative mobile charge in each period. Introduction of such a reservoir, implemented as a doped superlattice region is the key design innovation that led to the successful implementation of a unipolar laser. Subsequent QCL designs entrusted the reservoir with an additional mission to suppress the unwelcome tunneling from the upper level into the continuum. For this purpose, the superlattice is implemented as an electronic Bragg filter with a stop band in the range of energies of upper level states (Faist et al. 1995). Thus, most carriers enter the QW only via the upper and leave only via the lower subband, while leakage from the upper subband directly into the reservoir is negligible.

We have carried out a theoretical analysis of the QCL operation (Gelmont et al., 1996; Gorfinkel et al., 1996). This analysis will not be reproduced here; instead we confine ourselves to a brief discussion.

0-7803-4059-0/97/$10.00

Our analysis suggests that QCL operation is dominated by hot-electron effects. Non-equilibrium electron distributions arise from the power $\mathcal{P} \approx J \cdot \hbar\Omega$ per unit area, dissipated in each cascade period. The energy is stored in the *transverse degrees of freedom*, corresponding to in-plane motion of carriers and it fundamentally changes the lineshape of intersubband resonance and the spectral characteristics of gain. Transverse relaxation of the intersubband resonance and the hot-carrier effects are indispensable for the correct physical understanding of the temperature behavior of quantum cascade lasers.

Conventional two-level model does not adequately describe the intersubband gain function in experimentally realized QCL heterosystems. The reason is two-fold. Firstly, one cannot neglect the nonparabolicity: its inclusion suppresses the peak gain value by more than an order of magnitude. Secondly, the relaxation rate of intersubband resonance, which is mainly due to transverse intrasubband scattering processes, is strongly dependent on electron kinetic energy, $\gamma = \gamma(E)$. Indeed, the rate of optical phonon scattering has a threshold nature: when $E > \hbar\omega_{op}$ it increases by nearly an order of magnitude due to the onset of intrasubband emission.

The generalized expression for the intersubband gain at an optical frequency Ω is of the form (Gelmont et al. 1996):

$$g(\Omega) = \frac{4e^2 |z_{12}|^2 m_2 \Omega}{\hbar^3 a\, c\sqrt{\kappa_\infty}} \int_0^\infty \frac{d\varepsilon\, \gamma(\varepsilon)\, [f_2(\varepsilon) - f_1(\varepsilon_1)]}{[\Omega - \Omega_\varepsilon]^2 + [\gamma(\varepsilon)]^2} \quad , \tag{1}$$

where Ω_ε is the optical transition frequency for the in-plane electron momentum $\hbar k = \sqrt{2m_2 \varepsilon}$, viz. $\hbar\Omega_\varepsilon \equiv \hbar\Omega_0 + \varepsilon_2 - \varepsilon_1$, where $\varepsilon_2 \equiv \varepsilon$ and $\varepsilon_1 = \hbar^2 k^2 / 2m_1$ are kinetic energies in the upper and lower subbands, respectively, characterized by the effective masses m_2 and m_1 and the distribution functions f_2 and f_1. The function $\gamma(\varepsilon)$ describes the transverse phase relaxation rate due to intrasubband scattering, both elastic and inelastic.

Depending on the laser design, there may be different scenarios of how this energy is distributed among various electrons and dissipated into the lattice. It is worthwhile to stress that Eq. (1) does not rely on the electron temperature approximation and remains valid for general electron energy distributions within each subband. Validity of Eq. (1) is not restricted to any particular scattering mechanism responsible for the transverse phase relaxation.

The most attractive situation arises at low carrier concentrations ($n_D \ll 10^{11}$ cm^{-2}) when electron-electron collisions are not fast enough to establish a common electron temperature T_e between the two subbands. It turns out that in this regime the lower-subband electron distribution can be approximately characterized by a negative temperature,[1] so that states near the subband bottom are mostly unoccupied. At the same

1. For high positive temperatures the electron distribution becomes uniform over the entire subband. For $T_e < 0$ the distribution is inverted, the lower energy states having smaller occupation probability; one can say that negative temperatures are higher than $T_e = \infty$,

time, the upper subband remains approximately in a thermal ensemble, characterized by the ambient temperature. This situation is most favorable for high gain. It is even possible to achieve high positive values of $g(\Omega)$ at room temperature without an overall population inversion between the two subbands. Within the framework of our theory, the low concentration regime can be treated rigorously.

For higher (but still moderate, $n_D \lesssim 10^{11}$ cm^{-2}) concentrations, the T_e approximation becomes applicable, but it is still possible (at least semi-quantitatively) to regard optical phonon scattering as the dominant phase breaking mechanism. In this range, we predict a peculiar hot electron effect, manifested in the dependence of the lasing wavelength λ on the pump current, including a regime where λ switches "digitally" between two stable values.

Very high concentrations ($n_D \gg 10^{11}$ cm^{-2}) require a special consideration, as it becomes necessary to explicitly include electron-electron scattering in the calculation of $\gamma(\varepsilon)$. Also the energy balance equation in this range should include the dependence of the electron cooling rate on the carrier density and effective temperature due to optical phonon bottleneck. Moreover, as shown by Warburton et al. (1996), at high carrier concentrations the nonparabolicity is strongly suppressed by depolarization, so that intersubband resonance becomes a collective effect. Our theory does not directly apply to the high-concentration limit.

Experimentally reported QCL heterostructures (Faist et al. 1994-1996) operate neither in the high-concentration nor in the low-concentration regime. For moderate concentrations our theory provides a semiquantitative account of all experimentally observed features, such as the existence of a sharply defined critical temperature beyond which the QCL does not reach the generation regime. This is due to the fact that the subthreshold gain is not a monotonic function of the injection current in QCL but reaches a maximum and then declines due to the hot-carrier effect. Above threshold, the dependence of gain on T_e leads to a lower than expected slope efficiency of the laser.

At moderate concentration it is also possible to have a positive gain even in the absence of inversion between the two subbands, i.e. for $n_1 \gtrsim n_2$. This effect, recently observed by Faist et al., occurs owing to the non-parabolicity ($m_2 > m_1$). At a sufficiently high wavevector k, the occupation probability of state $\varepsilon_2(k)$ in the upper subband is higher than that of state $\varepsilon_1(k)$, even though the lower subband has higher overall population. This can be also seen in a different way: in the regime, where both subbands are characterized by the same effective temperature, it is possible to introduce the subband quasi-Fermi levels E_{F1} and E_{F2} for the distributions f_1 and f_2, respectively. One can then show that the range of $g(\Omega) > 0$ corresponds to the relation $\hbar\Omega < E_{F2} - E_{F1}$, familiar from the theory of conventional semiconductor lasers (Bernard and Duraffourg, 1961).

In contrast, the existence of a positive gain for $n_1 > n_2$ at low concentrations does not depend on the nonparabolicity and is a much stronger effect predicted in our theory. The low concentration regime offers possibility of higher performance, because the carrier heating effects in this case actually improve the effective population inversion for states participating in the lasing transition.

Given the tremendous applications potential of the QCL, we believe the device deserves a major development effort. The improvement strategies that have born most fruit so far, have dealt with the kinetics of subband population and with the laser engineering, such as improved heat sink, cavity design, etc. We have identified three new strategies. First, one should strive to reduce the effects of non-parabolicity by employing new material systems and designs to engineer subbands with approximately equal kinetic masses in the QW plane. Next, one can attempt to reduce the carrier heating effects by introducing new carrier cooling channels, e.g., via intervalley phonon emission in the doped reservoir region. Third, one can render hot-carrier effects harmless by implementing the low concentration regime of operation. Our work shows that the QCL still has an enormous reserve for improvement.

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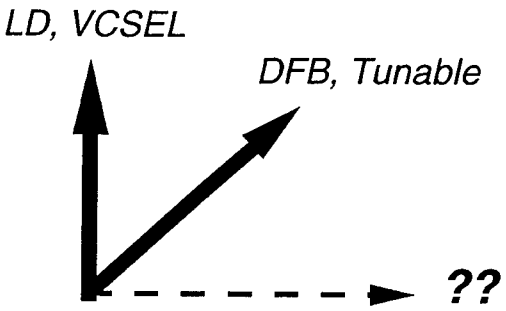
Exploring the Lateral Degree of Freedom in Semiconductor Lasers



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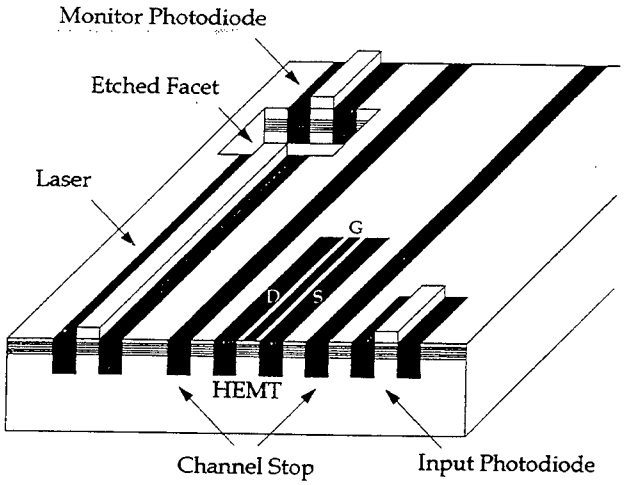
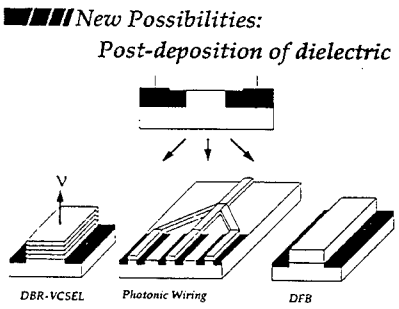
THE IDEAL ACTIVE SOURCE FOR MONOLITHIC OEIC should be grown on semi-insulating substrate for low parasitic conduction and delays; consist predominantly of undoped layers for easy of inter-device isolation and low free-carrier induced absorption and chirping; have both electrodes on the surface for easy of interconnection; and be readily fabricated using a planar process with a minimum number of steps.

Vertical injection lasers, though their performance as discrete devices is greatly perfected and presently enjoying the monopoly position with no competition in sight, are largely laterally invariant and do not generally possess these characteristics. A recent example is a demonstration of an integrated heterodyne receiver that required 150 processing steps (e.g., [1]). Conversely, lateral current injection lasers are natural candidates for integration, but remain to be studied systematically and developed to become a serious contender in the field.



EASY OF INTEGRATION IS ONLY ONE FEATURE of the great potential of the lateral injection lasers which results from the release of an additional degree of freedom.



For example, the use of non-conducting cladding layers enables capacitive modulation and gain and/or wavelength tuning from a top electrode.

Post-fabrication processing via deposition and modification of dielectric on a base structure allows us to add and extract different functionalities, which too is enabled by the absence of vertical injection through the layers. The use of the lateral degree of

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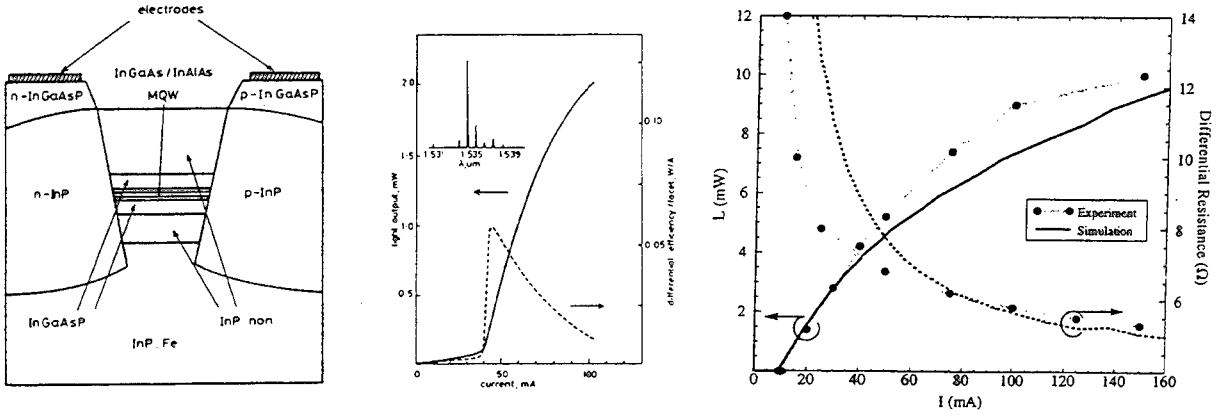
freedom reduces or removes the need for compromises between the electrical and optical design considerations which exist in the vertical paradigm. One benefit of this decoupling between the electrical and optical designs is that large bandgap undoped materials can be used in cladding and barrier layers to enhance both optical and electrical confinements without inducing extra resistance , heat and carrier non-uniformity and with reduced chirping.

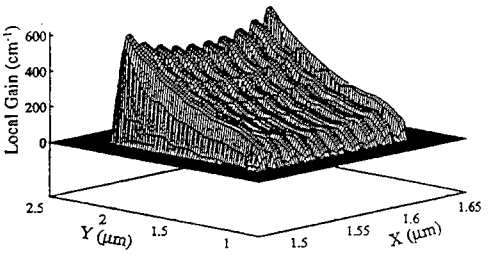
IF ONE MAY EXTRAPOLATE from the rate and richness of progress in the more constrained paradigm of vertical injection lasers, the exploration of an additional degree holds great promise for both improved performances in normal laser operation modes and new device possibilities in addition to the prospects of integration.

ATTEMPTS TO DATE (e.g.,[2-6]) in developing lateral injection lasers, despite the great potential, have yielded disappointing results, when compared with the highly developed and well understood vertical counterpart, with higher threshold current, lower output efficiency, earlier roll-off and lower maximum power. This situation, which is a result of the combination of scattered efforts and predominantly empirical adoptions of conventional laser designs, has impeded the further development of this class of lasing sources.



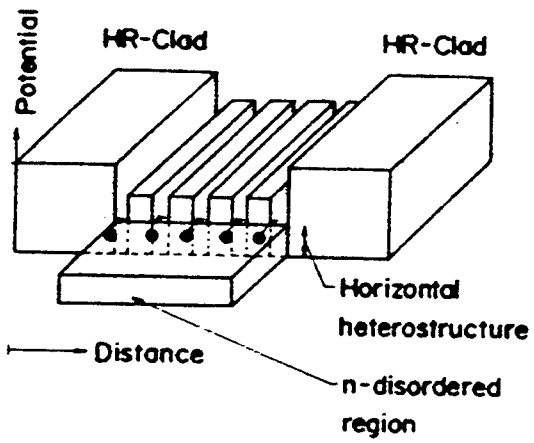
TO BE ABLE TO COMPETE with the vertical injection lasers on the front of pure performance in the conventional operation modes, and to realize its greater potential in novel functionalities and in integration, the lateral injection lasers should be given the same benefits of countless cycles and iterations of experiments informed by detailed theoretical studies.

A FEW THEORETICAL STUDIES (e.g. [7-10]) we have conducted so far reveal that the inner operation mechanism of the lateral injection lasers critically differs from that of the vertical ones in several aspects. These include: a large lateral asymmetry in the gain profile that results from the disparity

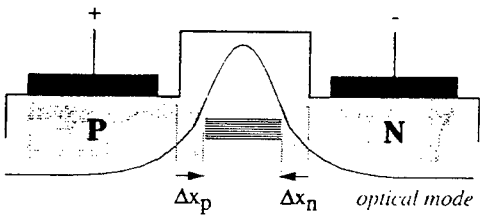


Simulated gain profile showing non-uniformity due to electron and hole mobility differences for an InP–InGaAs–InAlAs MQW LCI laser [5]. In the plot, 10 QW's are contacted by an n-type regrowth at $Y = 1.0$ μm and a p-type regrowth at $Y = 2.2$ μm. The effects of spatial hole burning in X and Y are also visible.

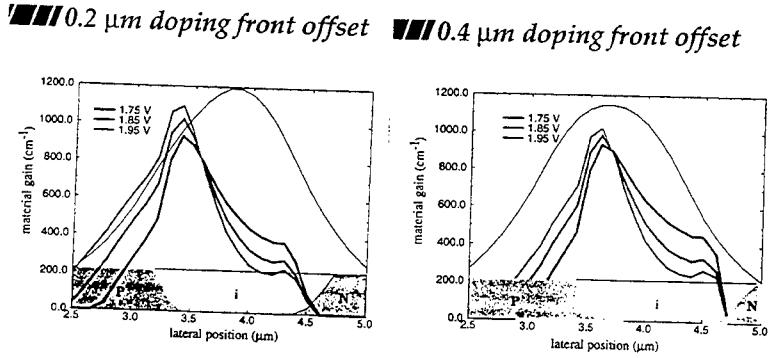
between electron and hole mobilities.; an under-or un-explored ambipolar carrier transport and heating process along QW planes; and a 3D-2D in-plane, as opposed to normal-to-plane, injection and capture process; and the many three-terminal laser-transistor operation mechanisms such as those involving capacitive modulation of bipolar current in the presence of stimulated recombination and those employing quantum Stark effects for gain and/or wavelength tuning, etc.



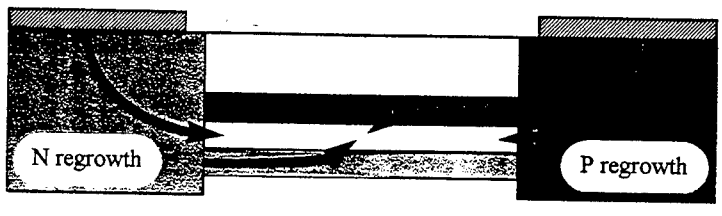
AND, IT IS ALSO FOUND that with a number of relatively minor but physically motivated changes to the existing designs and fabrication processes, lateral injection lasers can have greatly improved performance characteristics (as in the normal operation modes).
Doping profile engineering is one of the ways that are found effective in reducing the gain asymmetry and the resultant poor overlap between the gain and modal profiles.

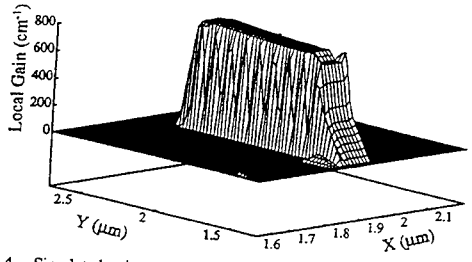


Doping profile engineering in a p-i-n lateral injection laser. Parameters describing the offsets of the doping fronts relative to the ridge are defined.



Incorporating current guiding in the barrier layers , thereby adding local later/vertical hybrid injection into the scheme, can also smooth the gain profile to the degree that is comparable to that of the pure vertical scheme.





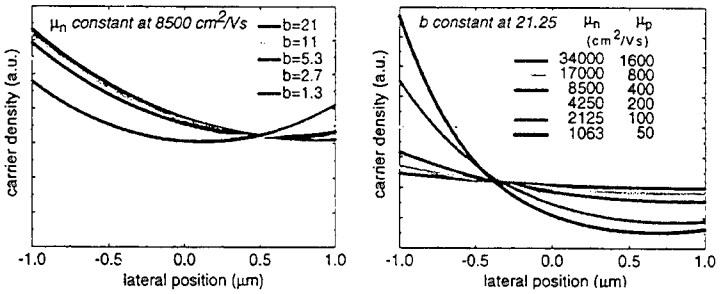
4. Simulated gain profile for an LCI laser with current guiding layers [6]. A 0.1-μm thick active region extends from the n-type regrowth at $Y = 1.5$ μm to the p-type regrowth at $Y = 2.5$ μm. The region above the active layer ($X < 1.8$ μm) is p-type and the region below ($X > 1.9$ μm) is n-type.

We have also shown that by reducing the mobility disparity or increasing both mobilities while keeping their ratio unchanged, one can also bring about a better gain-mode overlap. These may be achieved, in principle however difficult in practice, by introducing strain, strain compensation or cooling.

Carrier density profile: $\delta p \propto (b+1)\cosh\left(\frac{x}{L_i}\right)\cosh\left(\frac{d}{L_i}\right) - (b-1)\sinh\left(\frac{x}{L_i}\right)\sinh\left(\frac{d}{L_i}\right)$

Mobility ratio: $b = \frac{\mu_n}{\mu_p}$

Ambipolar diffusion length: $L_i^2 = \frac{2b}{b+1} D_p \tau$



SOME OTHER FUNDAMENTAL ISSUES, we identified in addition to the gain asymmetry and its physical origin, are yet to resolved:

. In-plane carrier capture from 3D to 2D (lateral, could be made less inelastic or more adiabatic, via "tapering" or "grading" through ion-mixing for example).

. Carrier transit times (reservoir to center, vertical v.s. lateral, ambipolar environment).

. RC delay (the capacitance of a QW plane seeing from the end? And, its resistance?)

. Carrier heating and its locality ?

. Chirp (~0? no plasma outside QWs if carrier heating is local, loss/gain compensated)

. Capacitive modulation of bipolar current (in the presence of stimulated recombination)

. Upper limit of current density per well (v.s. Jmax at the contacts)

. Maximum power (similar to "BJT versus FET" ?)

. Balance between reservoir spacing and mode size (waveguide width)?

This is a brief report on an on-going team work contributed by many, including Ted Sargent, Dave Suda, Alex Tager, and G.L. Tan, supported by Nortel, NSERC and OLLRC.

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EXPLORING THE FRONTIERS OF OPTOELECTRONICS WITH FIB TECHNOLOGY

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A review of the current and potential future uses of FIB technology for the fabrication of optoelectronic devices and circuits is presented. The advantages of the maskless and resistless FIB fabrication are briefly reviewed. A DBR laser totally fabricated by FIB (both gratings and channel waveguide) is discussed as an example of FIB-fabricated optoelectronic components. The opportunities and challenges of future applications of FIB technology in fiber-optic communications optoelectronics are considered. In this application, components such as WDM laser sources, add/drop filters, waveguides, and combiners can be ideally fabricated in an integrated optoelectronic circuit by FIB.

A. Introduction to FIB Technology

The applications of photon-based devices are expanding at a dizzying pace as displays, communications and computing are converting to sophisticated "man-image" interfaces as well as utilizing the trasmission of ever greater and faster optical data. As shown in Fig. 1, the parameter space defined by the axes of electronic signal processing, optoelectronic conversion, and optical signal processing contains single devices ranging from lasers to detectors to waveguides, as well as various photonic integrated circuits (PIC) and optoelectronic integrated circuits (OEIC).

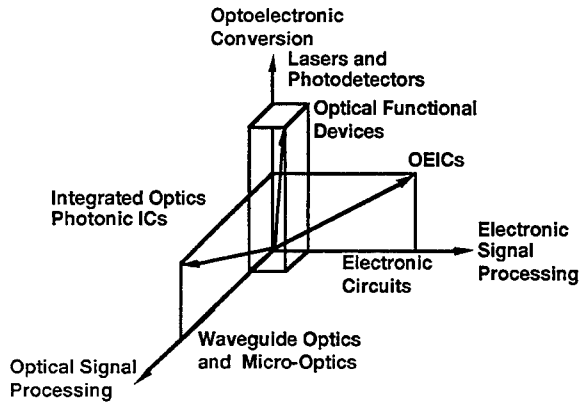

Fig. 1 Parameter space of optical function devices (after Wada and Crow[1]).

Most of the photon-based devices utilize compound semiconductors, with Si playing a minor role.Unlike Si digital integrated circuits, which deal with a single basic technology, photon-based devices cover not only a broad range of basic materials, but also require the development of different fabrication technologies for different applications. Focused ion beam (FIB) implantation is a maskless and resistless particle "beam" process[2], which can be applied with great versatility to the fabrication of optoelectronic devices. FIB micro- and nano-fabrication can be utilized to reduce the complexity required of conventional OEIC fabrication technology (in particular lithography, etching and implantation), which has to satisfy various requirements for different components fabricated on the same substrate.

FIB systems can provide an ion beam with a diameter ranging from a few μm down to ~10 nm. The focused ion beam is operated under computer control and can be placed on the sample surface with an accuracy equivalent to that of e-beam lithography systems using a laser interferometer driven stage. Since the focused ion beam combines energy, charge and mass in a single particle, FIB techniques for fabrication of optoelectronic devices include direct micromachining, maskless lithography, and implantation. The implantation approach accomplishes a certain functional aspect (usually charge carrier or photon confinement) of the device structure through the introduction of ions in order to provide either localized doping or ion-induced compositional mixing of multi-layer

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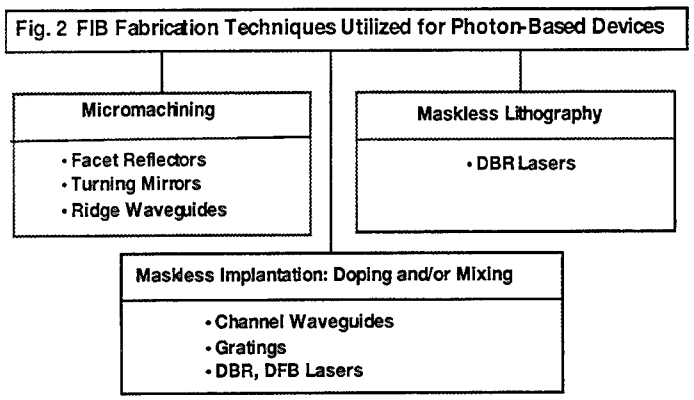
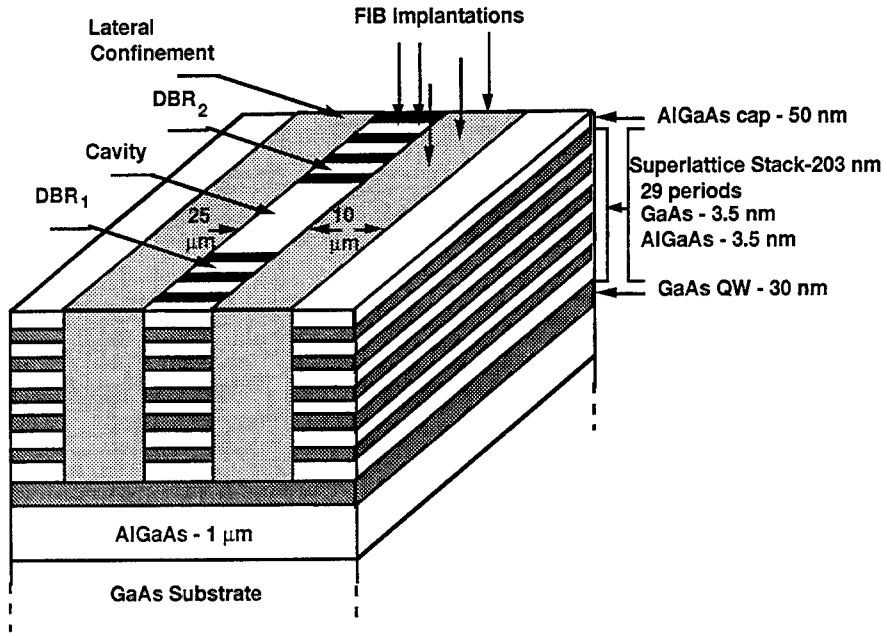
structures. In addition to being a high resolution maskless/resistless process, the FIB approach can readily adjust the implantation conditions (such as dose, energy, sometimes even species) in order to customize the process for each type of component during a single step.

B. FIB-fabricated Optoelectronic Components

FIB techniques have been used to fabricate various types of GaAs-based photonic and optoelectronic devices. Fig. 2 contains examples from each FIB fabrication approach. The examples range from mirrors fabricated by micromachining, to channel waveguides fabricated by mixing, to laser gratings fabricated by either doping, lithography or mixing.The fabrication of these devices by FIB has been recently reviewed by Harriott and Temkin[3] and by Steckl et *al.*[4] We have utilized primarily the mixing technique, wherein the FIB implantation of Si produces a localized region of much faster interdiffusion[5] of the Al in a $Al_{1-x}Ga_xAs/Al_{1-y}Ga_yAs$ superlattice upon thermal anneal. An important example is the fabrication of a DBR laser[6] by FIB mixing of superlattice/quantum well structures, as shown in Fig. 3. The FIB was utilized to fabricate both the gratings of the two distributed mirrors and the lateral confinement channel. The FIB mixing process utilized a ~70 nm diameter Si^{++} beam at an energy of 200 keV and a dose of 10^{14} cm^{-2}. The DBR grating period was 350 nm, designed to correspond to 3rd order emission from the 30 nm wide quantum well. The mixing technique was also succesfully utilized to fabricate[7] relatively long (~1 cm) channel waveguides in a similar superlattice structure.





The main characteristics of the DBR laser under optical pumping consisted of several very narrow modes (1.5 Å), a coupling coefficient of ~ 50-80 cm^{-1}, coupling efficiency of 1.75-2.8, and a maximum mirror reflectivity of nearly 80-90%.

Fig. 3

DBR laser structure.

C. Future Applications

A major potential application of FIB technology will be in producing integrated optoelectronics for future fiber optic communications. Operation of optical communications channels takes place at the near-IR minimum (~1.55 μm) of optical fiber absorption. The Er-doped amplifier is the first step in the evolution of fiber optic communications, as shown in Fig. 4. At the moment, the enormous bandwidth capacity of fiber optics is highly underutilized. To increase effective utilization of communication networks, wavelength or time multiplexing components need to be further developed. In turn this requires new capabilities on the part of optoelectronic technology. For example, utilizing the wavelength division multiplexing (WDM) method requires the fabrication of laser sources with very precise control over the emission wavelength in order to provide closely spaced (1-5 nm apart) channels in the 30 nm window operating window. This represents an ideal application for FIB technology for several reasons: (1) one can easily and accurately increment the wavelength by computer programming the period of the grating ; (2) one can adjust each design to account for *local* variations in the value of the refractive index; indeed, without FIB, one would need to hold variations in n to ~ 0.1%; (3) one can fabricate new designs with rapid turn-around due to the totally maskless and resistless nature of the FIB process. A simple prototype of an integrated WDM module is shown in Fig. 5. This circuit, which contains three closely spaced (both spatially and in emission wavelength) DBR laser sources and a waveguide combiner, can be fabricated by FIB implantation in essentially a single process step.

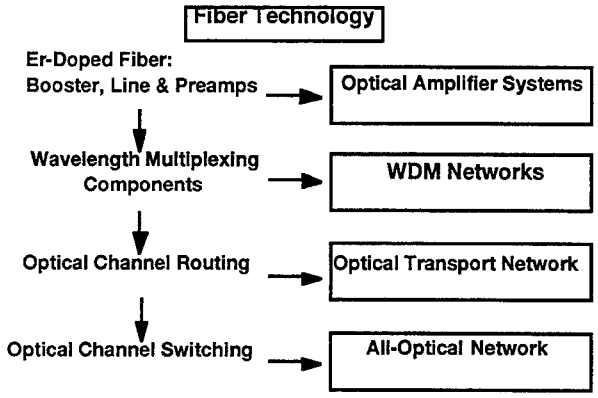


Fig. 4 Evolution of fiber optic communication.

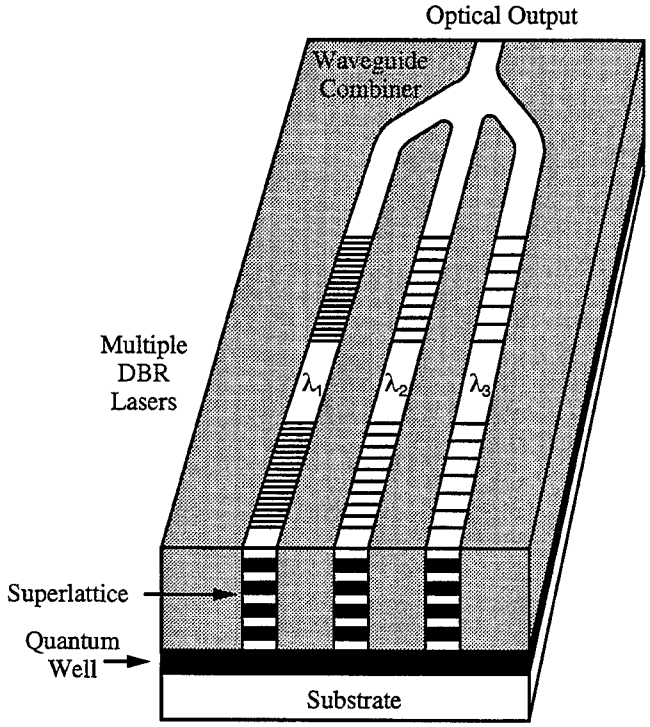


Fig. 5 Prototype of WDM module.

The next step in the evolution of fiber optic communication will include sophisticated optical channel routing and switching. A schematic implementation of such a circuit is shown in Fig. 6. This system uses WDM transmittters and receivers, Er-fiber amplifiers and add/drop filters. The latter are used to introduce new signals into the communication system, as well as to prevent their transmission past a certain location. In this system , most if not all all elements can be fabricated by FIB implantation. This includes the sources, the waveguides, the combiners, add/drop filters,

and the optical switches. This shows the enormous appeal of this fabrication approach for the future of fiber optic communications cicuits.

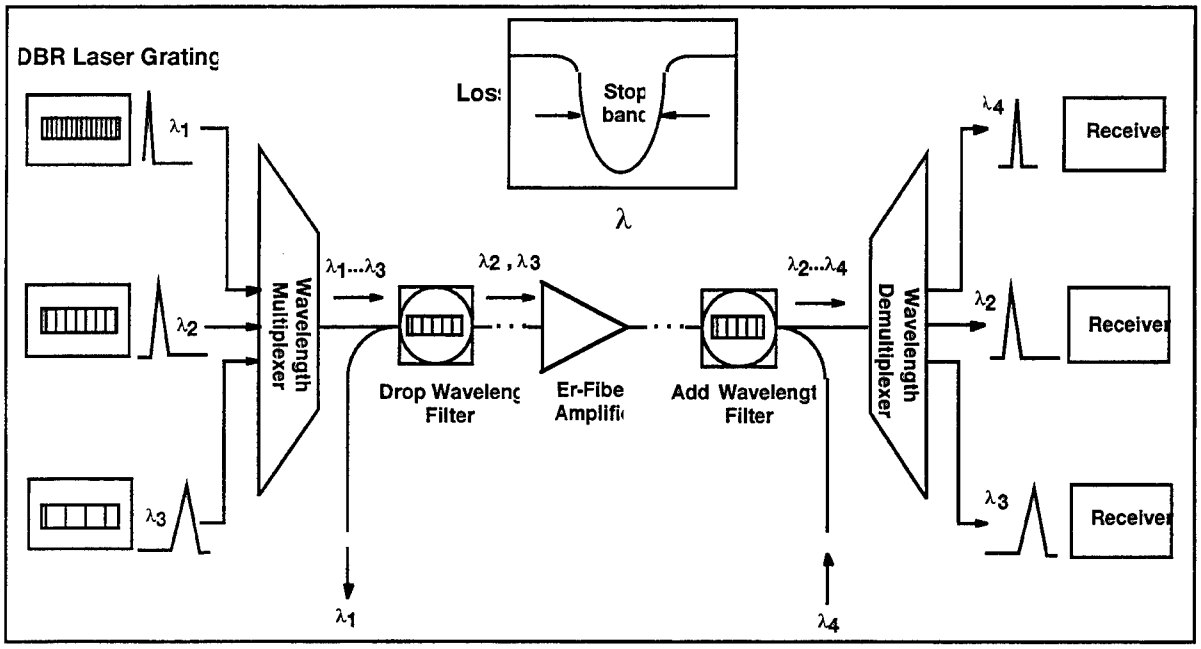


Fig. 7 A schematic diagram for a WDM-based fiber optic photonic system. The inset represents the generic stop-band spectral response of the add/drop filters.

D. Summary

In this article, I have briefly reviewed the potential future impact of a simple fabrication technology for optoelectronic and photonic devices and circuits based on focused ion beam implantation. In particular, I have explored the posibility of fabricating complex photonic circuits for fiber optic communications solely through the use of FIB implantation. The versatility and simplicity of this maskless/resistless process appears to render it quite attractive for such applications.

I would like to acknowledge the interaction and contributions at Cincinnati of my colleagues (J. T. Boyd and H. E. Jackson) and many former students (especially P. Chen, M. Kumar, and A. G. Choo). Support for this work from the National Science Foundation and the Materials Directorate, Wright Laboratory at the Wright -Patterson Air Force base is also gratefully acknowledged.

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PIEZOELECTRIC III-V SEMICONDUCTOR DEVICES

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Strained III-V layers develop a charge polarization vector for all orientations except for the standard (001) one. Besides, by selecting the crystal orientation, a valence band engineering can be made, to exploit sub-band splitting and their anisotropies. Piezoelectric devices have shown superior performances in modulators, SEED's and HEMT's. Besides, very low threshold current have been achieved in strained lasers when grown along orientations different from the (001). It has been shown that the piezoelectric electric field is only partially screened at lasing. Polarization control in VCSEL's, and double harmonic generation, have also been proposed as another areas of application for structures grown along non-(001) surfaces.

In the search for new and improved electronic and optoelectronic devices, engineers have develop different tools (materials/alloys, heterojunctions, quantum confinement), and recently strain was incorporated. Crystal orientation is as a new tool, and strained low-dimensionality structures grown along non-(001) orientations offer new and interesting possibilities. Although it was well known that III-V semiconductors were piezoelectric materials, the indication that strained III-V layers will develop very *important piezoelectric fields (PEF), except for the standard (001) orientation* was published about a decade ago [1]. In general, interface polarization charges, and hence piezoelectric fields, will be developed in strained structures along non-standard index surfaces (NIS), and they are maximum for growth along the (111) direction. For the InGaAs/GaAs systems, piezoelectric fields as large as 4×10^5 V/cm were predicted and experimentally confirmed [2].

In quantum confined structures, the use of pseudomorphically strained layers along directions other than (001), incorporate a number of potential benefits: a) the presence of built-in piezoelectric fields that can be controlled in sense and also modulated externally; b) a valence band structure with a larger HH-LH subband splitting, that leads to a lower in-plane hole effective mass density of states and to an enhancement of the TE polarization mode, and with a significant anisotropy that allows to control the in-plane polarization angle; c) a lower impurity incorporation (a reduced C concentration has been claimed for GaAs (111)B orientation); d) a dopant site incorporation that depends on substrate orientation and growth conditions, and that may lead to an enhanced amphoteric behavior of certain species; e) for these non-(001) orientations, the critical layer thickness may be larger than for the (100) orientation, allowing the growth of new pseudomorphic structures; and, f) for proper orientations, the presence of optical matrix elements that enhance the oscillator strength. Most of the experimental work on NIS has been made on GaAs-based structures, although the use of InP substrates is attracting a growing attention.

A basic structure to study the PEF fingerprints is to embed one or several strained QW's into the intrinsic region of a P-I-N diode (e.g. GaAs/InGaAs/GaAs (111)B). The optical edge

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absorption shows an intrinsic red-shift because the quantum-confined Stark effect (QCSE) due to the intense built-in PEF. By increasing the external reverse bias, the QW field decreases and a *blue-shift* of the optical transitions, that is close to linear with the field increment, is produced. The QW PEF can be screened by injected or photogenerated carriers (*in-well screening*). When analyzing piezoelectric P-I-N MQW diodes, calculations reflect that the PEF in the QW's depends on the structure design, and decreases as the number of wells increases [3]. An emerging new concept is the *average electric field* (AEF) in the MQW region. AEF can be positive (its sense is the same than the built-in junction field); can be flat (AEF=0); or can be negative (AEF<0, and the diode potential has a N-shape). The AEF is an important parameter for the P-I-N MQW electro-optical properties [4]. The structures with AEF<0 give rise to novel effects, as it will be described later. The AEF can be controlled by design and/or by the external bias, and in properly designed structures, we may go from an AEF>0 to an AEF<0 situation just varying the external bias. These ideas were also applied to piezoelectric SL's, allowing sub-band alignment and carrier sequential tunneling experiments [5].

Besides the generation of PEF, strained QW's grown along crystal orientations different from the (001) one, offer interesting novel optical properties. Considering first the valence band, the HH-LH splitting increases significantly for all orientations except for the (001), even without strain. Compressive strain helps *to reduce even more the in-plane effective HH mass, and thus the HH density of states*. As a direct consequence, the TE polarization mode is enhanced in the CB-HH transitions. Recent calculations point to an orientation-dependence of the optical matrix elements, and, for certain crystal orientations, the oscillator strength is enhanced affecting the optical gain. It has been shown that for growth along (001) and (111) directions, the in-plane optical gain is isotropic, while for the other growth directions there is a clear optical anisotropy that allows a *polarization angle selection mechanism.*

In pseudomorphic structures a very important parameter is the *critical layer thickness* (CLT). In III-V semiconductors, this problem was initially studied in (100) layers. For other orientations, there are changes in the elastic constants and in the dislocation geometry, and it was the hope that the CLT to be enhanced for certain growth directions. Several groups have considered the InGaAs/GaAs (111)B case, obtaining CLT values about twice than for (100) orientation (M&B model). A macroscopic relaxation study in InGaAs/GaAs single layers was conducted for (001) and (111) orientations, using DCXRD, PL, TEM and Raman scattering. For (111) orientations, relaxation is detected for thicknesses greater than *three times* the values for (001) direction [6].

The epitaxial growth along these NIS poses difficulties, and the level of understanding of the growth mechanisms is very limited. Most of the efforts have been made by MBE, and the growth on (111)A faces has been revealed as being much more difficult than on (111)B surfaces. On (111)B, the growth on "on-axis" substrates required a critical set of growth parameters. The use of misoriented substrates opened new possibilities [7]. In this case, growth proceeds by steps, and starts by nucleation at the step edges, being compatible with growth conditions on (001) substrates. Laboratories have been using various misorientation degrees and directions. As an example, high quality InGaAs/GaAs (111)B layers have been obtained at 500C using substrates 1°-off vs. the (2-1-1) direction, under a V/III flux ratio of 30. The growth of InGaAs/AlGaAs structures poses, obviously, more difficulties. In (111)B, dopants are well behaved, and a lower C incorporation has been reported. However, in (111)A and other high-

index orientations, dopant incorporation is more complex, with Si showing a clear amphoteric behavior [8].

Now that the physical bases for strained non-(001) orientation devices have been revised, let us consider their application areas. There is initially a set of structures designed to make use of their internal PEF. Modulators and SEED´s showing a blue-shift, and a better voltage sensitivity and contrast ratio than their (001) counterpart devices, were fabricated [9,10]. It was proposed that the PEF introduces non-symmetrical characteristics in (111)B DBRTD´s, and later confirmed experimentally [11,12]. In PIN-MQW devices with AEF<0, under illumination, new interesting effects are present. Because the special potential profile in the intrinsic region, photogenerated carriers tunnel and escape the QW´s, moving towards the extreme QW´s, creating a charge dipole that screens (out-well, long-range screening) the AEF. This spatial carrier separation is the source of memory, bistability, and negative-transient photocurrent effects [13,14].

Following early suggestions [1], a significant effort was placed to determine the non-linear optical absorption in (111) QW´s as compared with (001) structures. It was though that the in-well PEF screening by the photogenerated carriers, will produce larger optical non-linearities. It has been determined by various laboratories that the nonlinearities in the (111) samples were comparable, and not larger, than those in (001) samples [15]. Non-linearities due to out-well screening in AEF<0 structures have not been properly studied.

The benefits of the PEF in HEMT and HBT devices were early suggested [16]. In HEMT´s, the internal PEF will help to flatten the QW channel, allowing that the electron centroid to be farther from the interfaces, and thus the $\mu \times n$ product is cleraly enhanced [17].

Let us now consider strained non-(001) laser devices, where the PEF was not the source of the initial interest. The systematic study of (111)B AlGaAs/GaAs lasers by Hayakawa, showing very significant reduction of the threshold current for narrow QW´s, triggered the interest on non-(001) lasers [18]. For arbitrary crystal orientations, theoretical calculations of the VB were produced, pointing to the reduced in-plane HH effective mass as the main effect responsible for such J_{th} reduction in non-(001) lasers [19]. Very quickly, strained long wavelength non-(001) lasers were considered. Compressively strained, InGaAs lasers for 1.3μm and 1.5μm grown on NIS, with superior gain characteristics, have been reported [20,21,22]. Strain and crystal orientation were clearly responsible for a reduction of J_{th}. Polarization control is also offered by the use of NIS. It was indicated above that in (001) and (111) layers the optical gain is isotropic, while in (110), (221), (112) layers the VB has an in-plane lower order of symmetry, and a significant optical anisotropy was produced. Such anisotropy is used as a polarization-angle lock-in mechanism in VCSEL´s [23]. The advantages of NIS layers regarding polarization have also been used in DHG, to produce green-blue sources [24].

We can now consider the presence of PEF at lasing. To determine if the PEF is completely screened or not in the lasing QW, InGaAs/GaAs/AlGaAs (111)B GaAs devices were fabricated with standard parallel facets and with non parallel mirrors. In lasers, the subthreshold emission was blue shifted until lasing is reached, and then the emission wavelength is locked. In the non-lasing diodes the current density can be increased by a factor of four, and the electroluminescence emission keeps blue-shifting. This result indicates that the PEF is only

partially screened at lasing [25]. In this case, if we could modulate the laser gain (and thus J_{th}), a certain laser tunability may be produced by modulating the PEF through the injected carriers.

As a summary, the physics of PEF in non (001)-orientations is reasonably understood, the basic structures have been fabricated and analyzed, and our knowledge of the VB structure in strained QW´s for any crystal orientation has made a significant progress. There are still basic problems, ranging from the epitaxial growth and substrate selection to the determination of basic parameters, like the piezoelectric constant e_{14} , the CLT, hole effective masses, etc.. When considering applications, the direct use of PEF in devices has proven to produce improved modulators, SEED´s, HEMT´s, RTD´s, and charge storage effects due to the new achievable potential profiles in PEF PIN diodes. These improvements may not trigger yet the industrial interest for non-(001) substrates. It is in the area of lasers and optical sources where the use of strain and non-(001) substrates has produced significant advances in threshold current reduction, polarization control, and where novel applications of NIS are clearly foreseen (VCSEL´s, SHG). If the PEF present in these structures could be used to obtain new or improved device performances has not yet thoroughly investigated. Medium power InGaAs/GaAs (111)B, 1 to 1.3μm lasers, using the enhanced CLT available, and with a certain degree of tunability based in the modulation of the remaining QW PEF, is a suggested example for future applications of piezoelectric devices.

Is "*the non-(001) orientations*" a *Future Direction in Electronics?*. Clearly yes, in my opinion. By selecting the proper crystal orientation, the strain and the QW size, we have a powerful tool that combines symmetry considerations, valence band engineering and the presence of PEF.

Piezoelectric effects have also to be taken into account in III-V quantum wire and quantum box structures that involve the growth of strained islands, and the use of facets and strain fields. One may also indicate that in wurtzite GaN, strained layers grown along the standard (0001) axis will develop even larger polarization fields than in zincblende (111) GaAs.

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INFRARED IMAGING ARRAYS USING ADVANCED III-V MATERIALS AND TECHNOLOGY

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Photodetectors operating in the 3-5 and 8-12 μm atmospheric windows are of great importance for applications in infrared (IR) thermal imaging. HgCdTe has been the dominant material system for these applications. However, it suffers from instability and non-uniformity problems over large areas due to high Hg vapor pressure during the material growth. There has been a lot of interest in the use of heteroepitaxially grown Sb-based alloys, its strained layer superlattices, and GaAs-based quantum wells as alternatives to MCT. This interest has been driven by the advanced material growth and processing technology available for III-V material system.

InSb is a well established material system for mid-wavelength infrared (MWIR) applications including IR thermal imaging, environmental gas monitoring, and free space communications. InSb focal plane arrays (FPA's) have been well researched, but only on InSb substrates[1-4]. These substrates have several drawbacks and limitations. First, InSb substrates are limited in size because the quality is not uniform as the wafer diameter increases. In addition, InSb substrates are expensive, non semi-insulating, and are of lower quality than GaAs or Si. And most importantly, InSb substrates used for FPA's muse be thinned to ~ 10 μm for proper device operation due to absorption in the substrate. This thinning is a major yield-limiting step in the FPA fabrication process, and this problem is only exacerbated by the limited substrate size.

Thus the use of suitable alternative to InSb substrates is very attractive to InSb technology. GaAs, Si, and Sapphire are possible candidates despite having large lattice mismatch (4-15%). For these materials to be viable, the devices fabricated on them must have performance comparable to that of bulk arrays with the advantage of larger area arrays with excellent uniformity. Comparing the large lattice mismatch these materials have with InSb, especially GaAs, it would seem impossible that device performance could be anywhere near that of existing technology. However, in this paper we report on the first IR imaging obtained from InSb FPA's fabricated on GaAs or Si substrates with performance comparable to that of bulk InSb detectors.

InSb was grown on GaAs, Si, and Sapphire substrates using MBE growth technology[5-7] Optimum growth conditions have been determined and discrete devices have been fabricated on each substrate materials[8]. The structural, electrical, and optical properties were verified using x-ray diffraction, Hall, photoresponse, and photoluminescence (PL) measurements. Measured x-ray full width at half maximum (FWHM) were as low as 55 and 100 arsec for InSb layers on GaAs and Si substrates, respectively (Fig. 1). Hall mobilities were as high as 95,000 and 72,000 cm^2/Vs at 77 K and 300 K (Fig. 2). In addition, PL linewidths were as low as 18, 20, and 30 meV on GaAs, Si, and Sapphire substrates, respectively.

0-7803-4059-0/97/$10.00

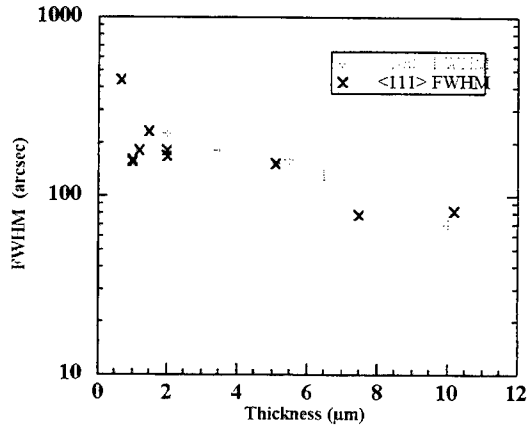

Figure 1. Measured X-ray FWHM of InSb layers on GaAs and substrates.

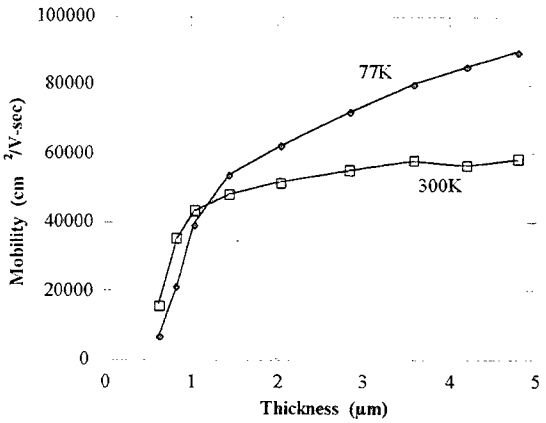

Figure 2. Measured Hall mobility of InSb layers at 77K and 300K.

The photovoltaic detectors were fabricated on GaAs and Si substrates. As shown in Fig. 3 peak voltage responsivity as high as ~ 10^3V/W was obtained with estimated detectivity of ~ 3×10^{10}cmHz$^{1/2}$/W. The first successful IR imaging from heteroepitaxially grown InSb on GaAs and Si substrates has been obtained (Fig. 4).

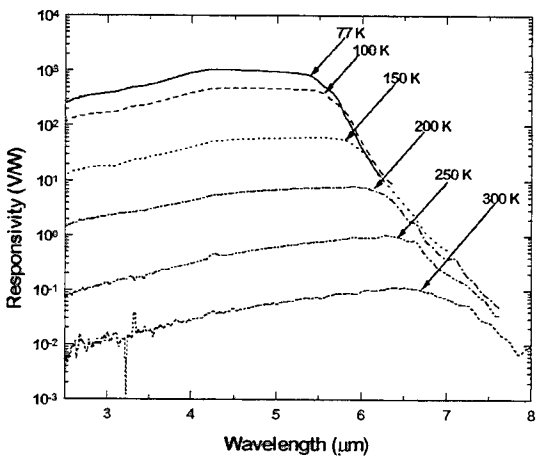

Figure 3. Spectral response of an InSb photodiode on (100) Si.

Figure 4. Infrared imaging from InSb focal plane arrays on GaAs substrates.

There has been considerable interest in InAsSb alloys and their strained layer superlattices for infrared detectors[9-16]. The inherent stability, well behaved donor and acceptor impurities, available low cost and high quality substrates, and advanced technology of InSb-based materials are expected to overcome the metallurgical problems of HgCdTe, the current leading material for long wavelength infrared detectors.

Earlier data suggested that InAsSb can exhibit a cutoff wavelength up to 12.5 μm at 300 K[9]. However, some recent experimental results demonstrated that the cutoff wavelength of epitaxial layers can be longer than 12.5 μm, thus covering the entire 8-14 μm at near room

temperatures[11,16]. This may be due to structural ordering[15], but the exact mechanism has not been determined yet. These results show that InAsSb is promising material system for long-wavelength infrared (8-14 μm) photodetectors operating at near room temperatures.

In this paper, we report InAsSb photodetectors operating in the 3-14 μm range without cryogenic cooling. The devices are InAsSb-based heterostructures grown on (100) semi-insulating GaAs substrates by low pressure metalorganic chemical vapor deposition (LP-MOCVD). Structural and electrical characterizations have been performed using high-resolution X-ray diffraction and Hall measurements, respectively. Infrared transmission and spectral response were measured using a Fourier Transform Infrared (FTIR) spectrometer. Absolute photoresponse is determined using 800 °K blackbody measurement setup.

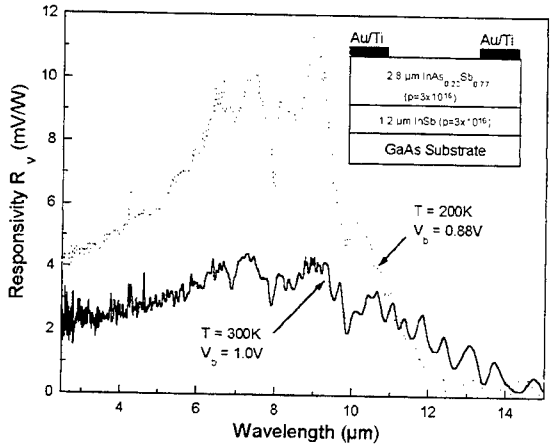

Figure 5. Spectral voltage responsivity of an $InAs_{0.23}Sb_{0.77}$ photoconductor at 200 K and 300 K.

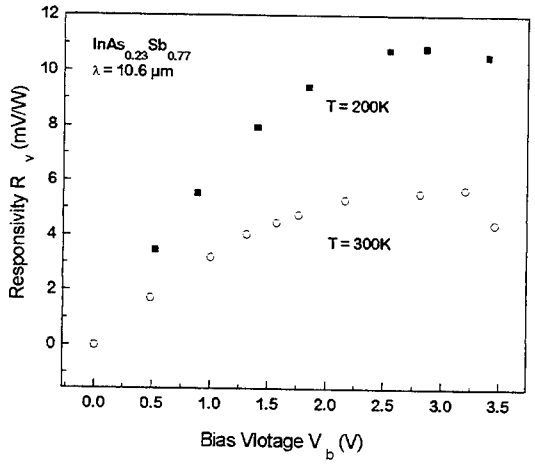

Figure 6. Voltage-dependent responsivity of an $InAs_{0.23}Sb_{0.77}$ photoconductor at 10.6 μm.

The photoconductive detectors are p-InAsSb/p-InSb heterostructures grown on GaAs substrates. Room temperature photoresponse up to ≈14 μm has been obtained in an $InAs_{0.23}Sb_{0.77}$ sample as shown in Fig 5. From the voltage dependent responsivity measurement, the effective lifetime of about 0.14 nsec has been obtained at 300 K (Fig. 6). The estimated detectivity at λ=10.6 μm is limited by Johnson noise at the level of about $3.27 \cdot 10^7$ $cmHz^{1/2}/W$ at 300 K, while the generation-recombination limit is $\approx 1.5 \cdot 10^8 cmHz^{1/2}/W$.

The photovoltaic devices consist of a double heterojunction of p^+-InSb/p-$InAs_{1-x}Sb_x$/n^+-InSb on (001) GaAs. The mesa structures have been prepared by photolithography and wet chemical etching. Au/Ti contacts were deposited by e-beam evaporation. The doping level and detector structures have been determined through theoretical calculations prior to the experiment.

Room temperature photovoltaic response up to about 14 μm has been measured with a $x \approx 0.85$ sample[17] (Fig. 7). The voltage responsivity-area product of $1.46 \cdot 10^{-4}$ Vcm^2/W and corresponding resistance-area product (R_oA) of $7.56 \cdot 10^{-5}$ Ωcm^2 has been obtained at 300 K for λ=10.6 μm as given in Table 1. At high temperatures, the R_oA products were close to the values set by Auger-limited processes, but they were far below the calculated values at low temperatures as is shown in Fig. 8. At low temperatures, the R_oA products are limited by generation-recombination process with different carrier lifetime.

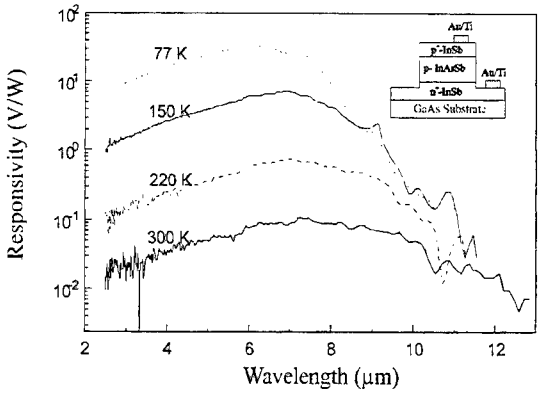

Figure 7. Spectral response of an $InAs_{0.15}Sb_{0.85}$ photovoltaic detector.

The normalized detectivity of the photovoltaic devices was limited by the Johnson-Nyquist noise due to a high series resistance and preamplifier noise. The generation-recombination limited detectivity at 300 K could be achieved only in extremely small ($\approx 20\ \mu m^2$) area devices.

The results show that p-InAsSb-based heterostructures have great potential for 8-14 μm infrared photoconductive and photovoltaic devices at near room temperature. Further improvements of the performance are expected be achieved by optimization of band gap and doping profiles, and by the use of non-equilibrium mode operation.

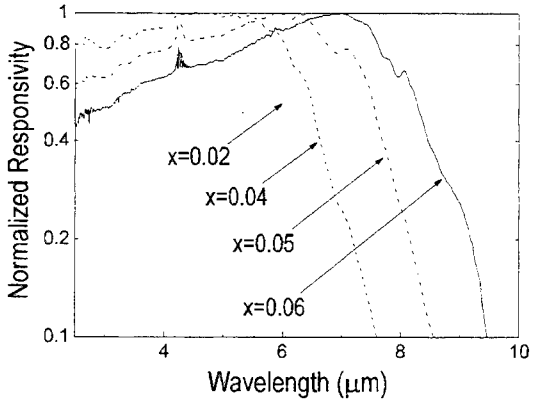

Figure 9. The normalized spectral response of the $In_{1-x}Tl_xSb$ photoconductors at 77 K.

Table 1. Responsivity-area product and resistance-area product of InAsSb photovoltaic detectors as a function of temperature.

T (K)	R_vA ($V\cdot cm^2/W$)	RoA (Ωcm^2)
77	4.56×10^{-2}	3.15×10^{-2}
100	2.58×10^{-2}	1.53×10^{-2}
150	9.68×10^{-3}	5.73×10^{-3}
200	1.64×10^{-3}	9.71×10^{-4}
220	1.03×10^{-3}	6.10×10^{-4}
250	5.57×10^{-4}	3.30×10^{-4}
300	1.46×10^{-4}	7.56×10^{-5}

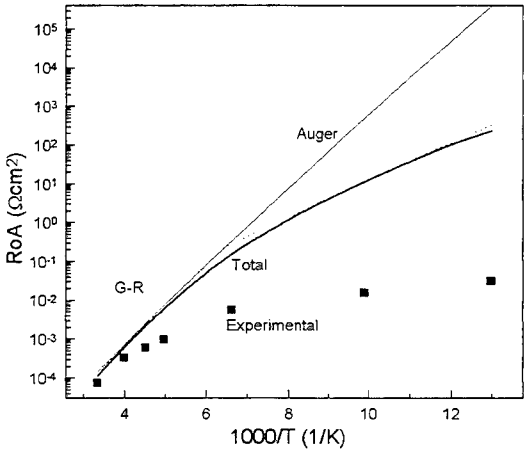

Figure 8. Comparison of experimental R_oA values with the theoretical limit.

As an alternative to the InAsSb material system, InTlSb was proposed as a potential infrared material at long wavelength[18]. The epitaxial growth of InTlSb on GaAs substrates using low pressure chemical vapor deposition (LP-MOCVD) has been reported[19,20].

We demonstrated room-temperature operation of InTlSb photodetectors with a cut-off wavelength of about 11 μm[21]. The photodetectors were grown on (100) semi-insulating GaAs substrates by low pressure metalorganic chemical vapor deposition (LP-MOCVD). The cut-off wavelengths of the

InTlSb photodetectors has been extended as the Tl composition increases (Fig. 9). As shown in Fig. 10 the cutoff wavelength has been increased up to 11 μm at room temperature. The maximum responsivity of an $In_{0.96}Tl_{0.04}Sb$ photodetector is about 6.64 V/W at 77 K, corresponding to a detectivity of about 7.64×10^{8} cm·Hz$^{1/2}$/W. The photoconductive carrier lifetime has been determined from the bias voltage dependent responsivity (Fig. 11). The carrier lifetime in InTlSb photodetectors derived from the stationary photoconductivity is 10-50 ns at 77 K.

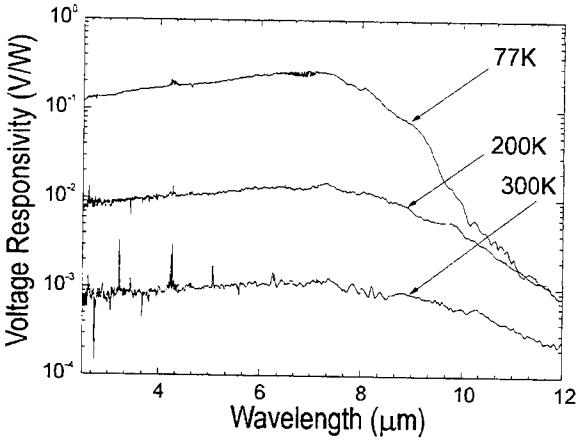

Figure 10. The spectral responsivity of an $In_{0.94}Tl_{0.06}Sb$ photoconductor at 77 K, 200 K, and 300 K.

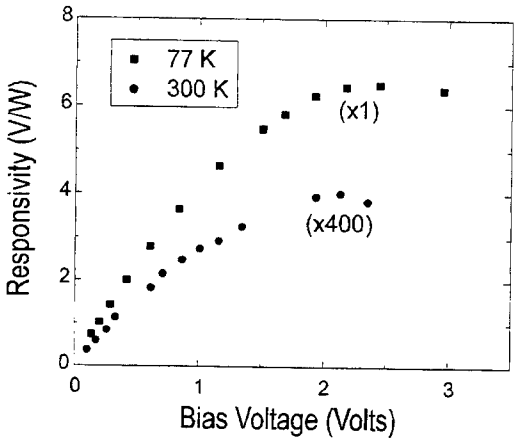

Figure 11. Voltage-dependent responsivity of an $In_{0.96}Tl_{0.04}Sb$ photoconductor.

As another alternative to the InAsSb material system, InSbBi has been considered because the incorporation of Bi into InSb produces rapid reduction in the bandgap of 36meV/%Bi[22]. Thus only a few percent of Bi is required for the desired reduction in the bandgap energy. There have been various efforts to grow InSbBi using different growth techniques such as Czochralski[23], multitarget sputtering[24], molecular beam epitaxy (MBE)[25,26], and metalorganic chemical vapor deposition (MOCVD)[27,28].

In this paper, we report the successful growth of InSbBi alloys and fabrication and characterization of photodetectors. The layers were grown on (100) InSb substrates by low pressure metalorganic chemical vapor deposition (LP-MOCVD). Fig. 12 clearly shows the two separate peaks responsible for InSb and

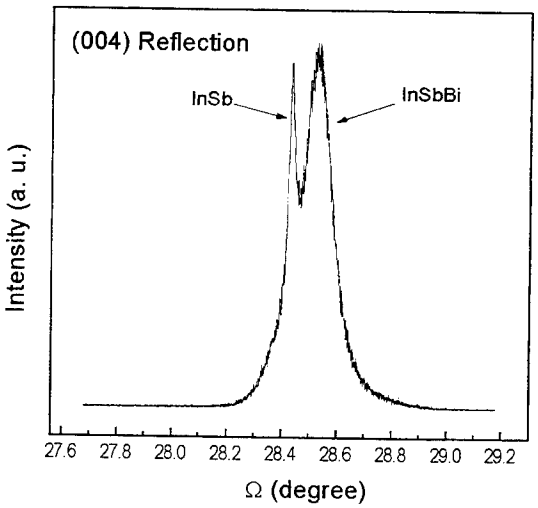

Figure 12. X-ray diffraction spectra of InSbBi layers grown on InSb substrates.

InSbBi. The cut-off wavelengths of the InSbBi photodetectors has been extended as the Bi incorporation increases as shown in Fig. 13.

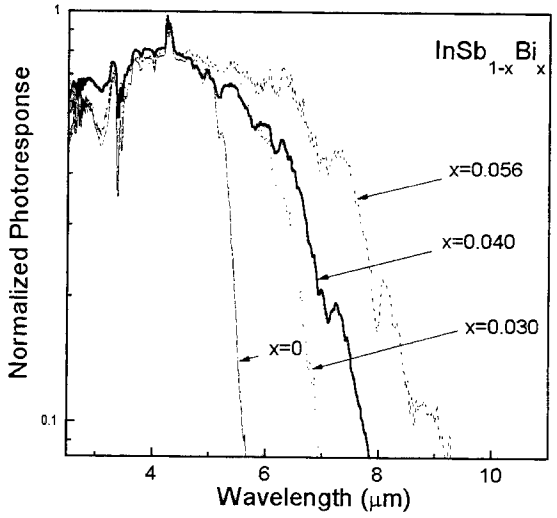

Figure 13. Normalized photoresponse of $InSb_{1-x}Bi_x$ alloys for various Sb compositions.

Multispectral infrared detectors arrays with response in both 3-5 and 8-12 μm regions corresponding to the two on atmospheric "windows" of decreased absorption are useful for focal plane array imaging applications. Infrared detectors in the long wavelength range (8-12 μm) have been produced using intrinsic semiconductors such as $Hg_{1-x}Cd_xTe$ and $Pb_{1-x}Sn_xTe$[29], in which the energy gap can be controlled by varying x. However, these low band gap materials are characterized by weak bonding and low melting points, and are more difficult to grow and process than large-band gap semiconductors such as GaAs.

These problems have lead to the development of quantum well infrared photodetectors (QWIPs) based on intersubband transitions in multi-quantum well (MQW) structures of AlGaAs/GaAs[29], GaInP/GaAs[29-31], and AlInAs/InGaAs[32].

Recently we have demonstrated lattice matched p-type GaAs/GaInP QWIPs operating in the mid-wavelength infrared (MWIR) spectral range ($\lambda \sim 3\text{-}5$ μm)[30-31] (Fig. 14). This is in contrast to the short wavelength limit of 5.6 μm in the GaAs/AlGaAs material system[29] imposed by keeping a direct bandgap in the AlGaAs barrier material.

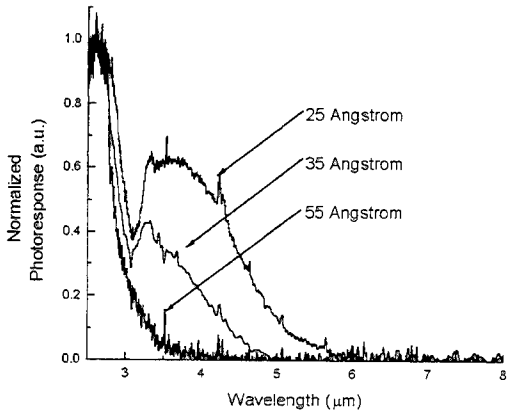

Figure 14. Normalized optical response at 77K for *p*-QWIPs with 25Å, 35Å and 55Å quantum wells.

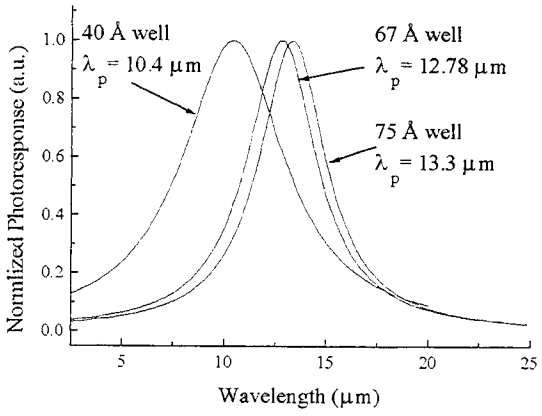

Figure 15. Normalized optical response at 77K for samples with 40Å, 65Å and 75Å quantum wells.

In this letter, we also demonstrate longer wavelength quantum well infrared photodetectors based on a *n*-type GaAs/$Ga_{0.51}In_{0.49}P$ superlattice structure grown by gas-source molecular beam epitaxy. Wafers were grown with varying well widths. Wells of 40Å, 65Å, and 75Å resulted in peak detection wavelengths of 10.4, 12.8, and 13.3 mm with a cutoff wavelength of 13.5, 15, and 15.5 mm respectively (Fig. 15) The measured peak and cutoff wavelengths match those predicted by eight band theoretical analysis (Fig. 16). As shown in Fig. 17, the measured dark currents were lower than equivalent GaAs/AlGaAs samples.

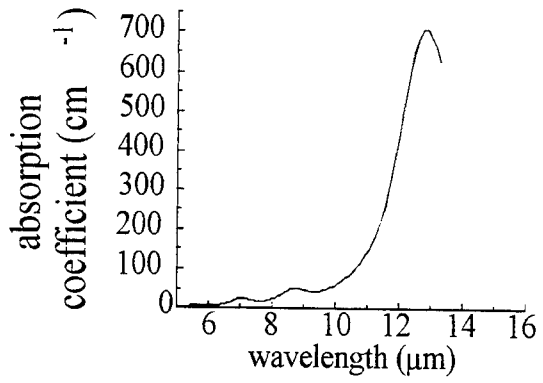

Figure 16. Calculated absorption spectrum for 75Å GaAs / 500Å GaInP superlattice.

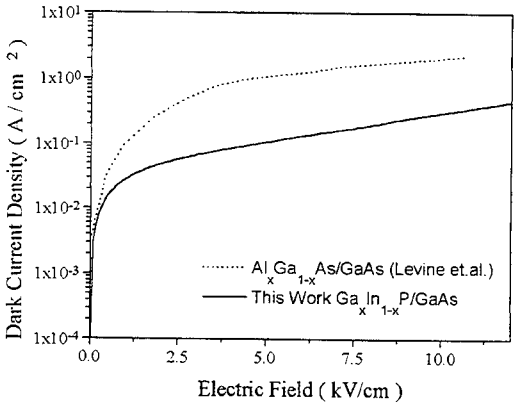

Figure 17. Comparison of 77K dark current for the sample with 65 Å quantum wells with the results of Levine et.al. J.Appl.Phys. **70** 5101 (1991).

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Design and characterization of Two Color GaAs based Quantum Well Infrared Detector structures

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Abstract. The choice of detector technology for Infrared focal-plane arrays may be influenced by several factors as sensitivity, uniformity, array size, reproducibility, cost and integration posibilities. The material system GaAs/AlGaAs provides several advantages compared to the state-of-the-art II-VI semiconductor detectors, including the mature GaAs growth and processing technologies and the flexibility of energy band tailoring in QW's to operate at different atmospheric transmission windows. In this work we report the detailed design procedure of a tunable two-color photoconductive GaAs/AlAs/AlGaAs and GaAs/AlGaAs stacked Quantum Well Infrared Photodector (QWIP). The structures are optimized to operate in the 3-5 μm [1] and 8-10 μm [2] windows, with peak detectivities at ~ 4 μm and 9 μm, respectively. A transfer-matrix method was used to estimate the subband energies of the structures according to the operating wavelength specifications. The effect of many-body corrections was also taken into account.

This work describes the main steps followed in order to develope a two color Quantum Well Infrared Photodetector. The characteristics of this design are the following:

Absorption ranges:	3-5 and 8-12 μ.
Detectivity:	$>10^{10}$ cm·√Hz/W

Design:

There are mainly three types of structures to choose in order to fabricate a QWIP. They are represented in fig.1. The first one is called bound to bound, the second one is called bound to continuum, and the third one is called bound to quasi-continuum. Each one has its advantages and its drawbacks.

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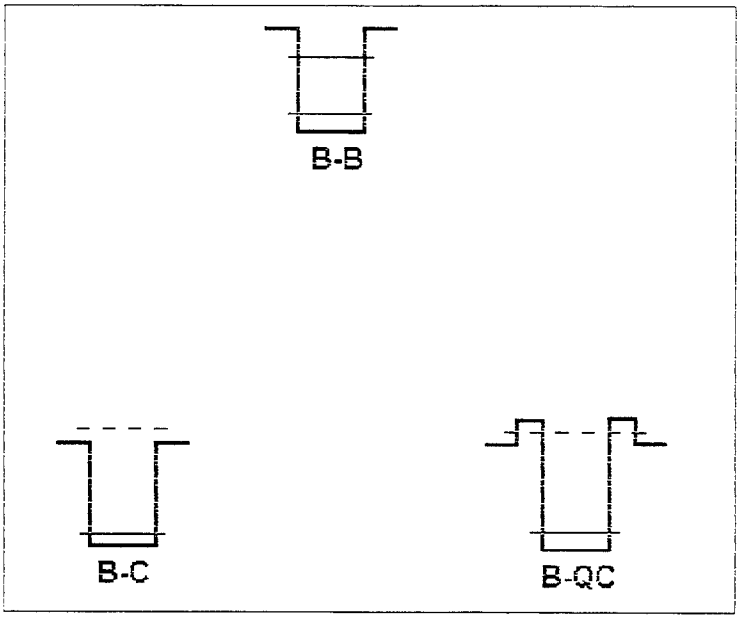

Fig 1. Three types of QWIP

The structure chosen for the device proposed in this work is the bound to quasi-continuum one. In this case, both the escape probability, and the quantum efficience can be adjusted in a more flexible way. The high energy level is partially confined by the thin lateral barriers.

The main expressions to be considered in the characterization of this QWIP, expressed in terms of basic magnitudes are the following [3]:

RESPONSIVITY

$$R_P = \frac{q}{E_2 - E_1} \cdot \eta_a \cdot p_e \cdot g$$

η_a = quantum efficience

p_e = escape probability

DARK CURRENT

$$Id(V) = q \cdot A \cdot n^*(V) \cdot v(V)$$

L_p = superlattice length

T(E) = transmission coefficient

f(E) = carrier distribution.

$$n^* = \frac{m^*}{\pi \cdot \hbar^2 \cdot L_p} \int_{E_1}^{\infty} f(E) \cdot T(E) \cdot dE$$

DETECTIVITY

$$D^* = \left(\frac{\eta_a \cdot p_e}{2 \cdot (E_2 - E_1)} \right) \left(\frac{\tau_L}{n^* \cdot l} \right)$$

τ_L = carrier lifetime

l = length of active zone

Here, we can see that the two main features of a QWIP are the position of the confined levels, and the transmission coefficient of the structure. These are the parameters that have been obtained by simulation.

To simulate the structure, we have used two numerical methods: the transfer matrix method, and the finite element method. The first one allows us to calculate the transmission coefficient and the second one, allows to calculate the position of the levels and the form of the wavefunction. This results are corrected by Self-consistent Hartree calculations, exchange and correlation effects and plasmon shift and exciton like effects [4].

The final structures are schematically shown below:

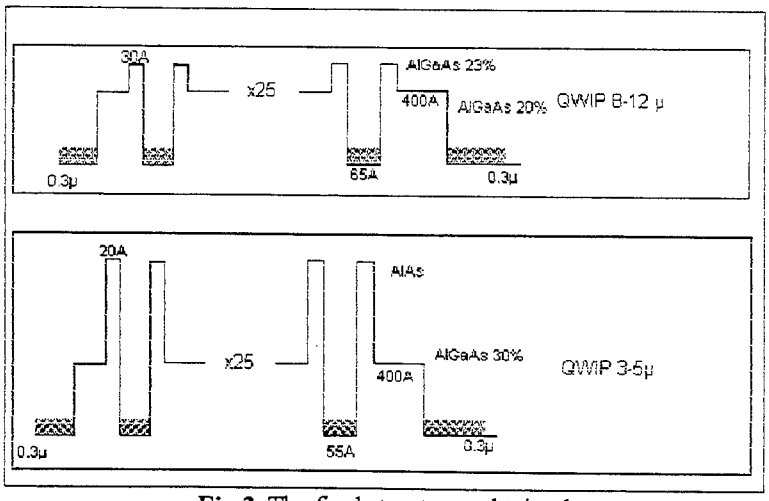

Fig 2. The final structures obtained

Both samples are grown by Molecular Beam Epitaxy and processed to obtain diodes with a "mesa" etching and ring contacts in the upper part of the wafer to allow optical access.

Characterization:

Before growing the final structures, we have selected a batch of samples in order to estimate the parameters of the devices and the quality of the MBE growth. This samples are described below:

Sample	Characteristics
#592,#612,#613	10 QW GaAs/AlGaAs 30% 100/200Å
#618	20 QW GaAs/AlGaAs 22% 65/400Å
#623	QWIP 8-12µ B-C, doping=2e18 cm^{-3}
#624	QWIP 3-5µ B-C, doping=2e18 cm^{-3}
#631	QWIP 8-12µ B-QC, doping=2e18 cm^{-3}
#632	QWIP 3-5µ B-QC, doping=2e18 cm^{-3}

Optical characterization:

The first samples, were grown in order to calibrate the optimum growth temperature. In the following plot, we can see the photoluminiscence spectra of three samples grown with different growth temperatures. Here we can appreciate that the PL intensity has approximately the same value for both samples #592 and #612. We have chosen 630°C as the growth temperature.

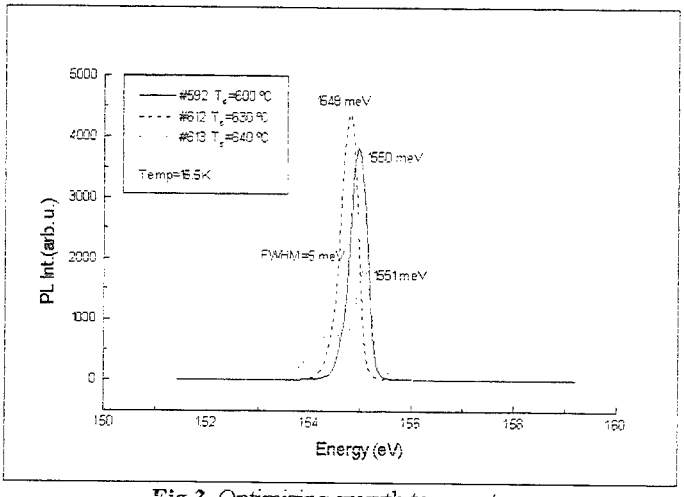

Fig 3. Optimizing growth temperature

Figure 4, shows the evolution with temperature of the photoluminiscence spectrum of a sample with the configuration of the 8-12 μ of absorption wavelength, but without the lateral barriers and whithout doping into the wells. We can see here, the peak associated with the main transition between the first electron level and the first HH level, and a peak associated with the transition between the electron level and the LH level. We can also observe, that this sample gives luminiscence signal at room temperature.

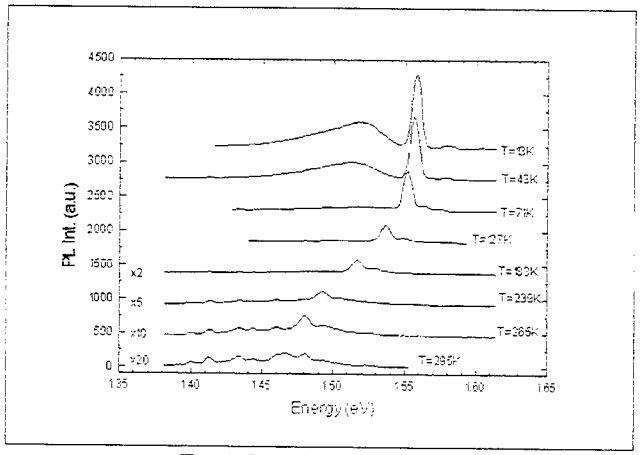

Fig 4. Sample #618

Figure 5, shows the full QWIP in the configuration of 8-12 μ. We can see here, the peak associated with the main transition between the first electron level and the first HH level, with a little shoulder that can be due to the presence of the Fermi level at an energy 40 meV higher than the main peak [5].

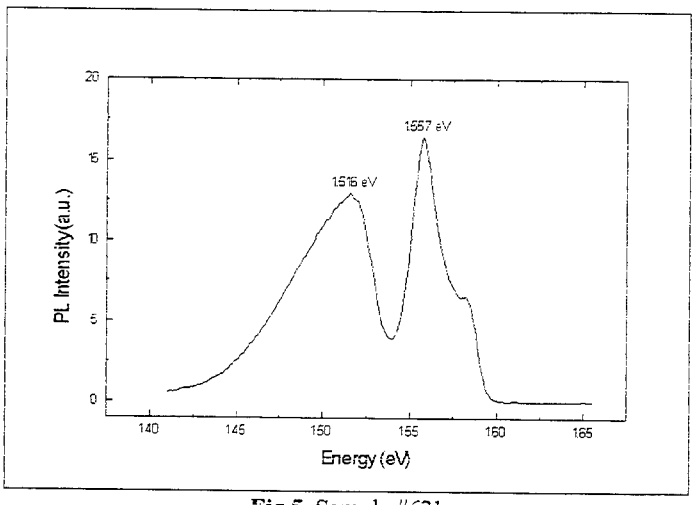

Fig 5. Sample #631

Electrical characterization:

In order to further evaluate the characteristics of our samples, we have performed different types of electrical measurements.

We know that the behaviour of the dark current follows the expresion [3]:

$$\frac{I_D}{T} \alpha e^{\frac{E_C - E_F}{kT}}$$

In fig 6, we plot the logarithm of the dark current divided by the temperature versus the inverse of the temperature. This Arrhenius plot, shows the difference between the cutoff frecuency and the position of the Fermi level. The extracted value for E_C-E_F is lower than expected. This may be caused by the presence of some kind of impurity in the interface between the AlGaAs and the AsGa layers which would give aconsiderable contribution from non-resonant tunnelling [6].

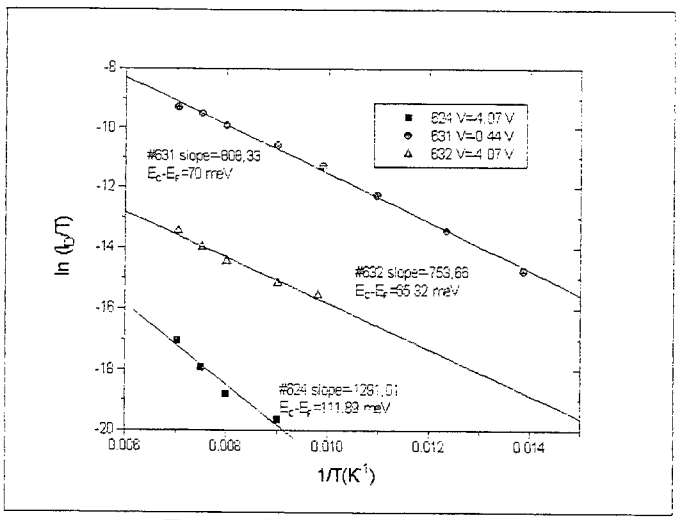

Fig 6. Dark current vs. temperature

In order to locate the position of the second confined electron level, we have performed photocurrent measurements, using a tunable laser and scanning all the energy range of the conduction band discontinuity. The result of this measurements, are presented below. We can see the feature corresponding to the onset on absorption at the Fermi level, and the transition related to the second electron confined level. The difference between this second level and the first one seen by photoluminiscence is the expected in this case.

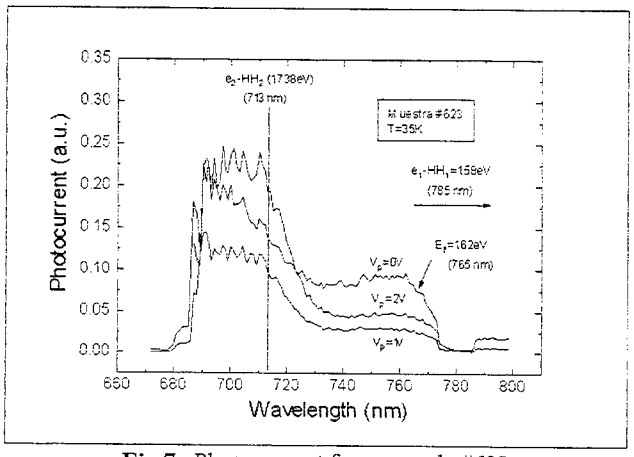

Fig 7. Photocurrent from sample #623

Summary:

- We have designed two quantum well infrared detectors with a range of absorption between 3-5μ and 8-12μ.

- Preliminary test structures have been grown by Molecular Beam Epitaxy on (001) GaAs substrates.

- Photoluminiscence and photocurrent spectroscopies have been applied to this device structures.

- Experimental transition energies are in good agreement with the calculated values.

- Next is to stack this two devices and to check the detectivity at both wavelengths.

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EPITAXIAL PHOTOCONDUCTIVE DETECTORS : A KIND OF PHOTO-FET DEVICE

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ABSTRACT: In epitaxial layers with a large area to thickness ratio, surface and interface space charge regions being modulated by the incident light, behave as transverse Resistance-Capacitance systems modulating the effective volume that takes part in the layer electrical conductivity. Photoconductivity spectroscopy has been applied to gated and ungated GaAs samples, to validate present model. We also show that any sample conductivity variation due to the photoconductive effect (carrier concentration variation due to light absortion) is largely exceeded by the volume modulation effect due to the width variations of the space charge regions. Implications for optoelectronic characterization techniques are discussed.

I. INTRODUCTION

A photoconductive technique being used to study carriers and traps in semiconductors, the so called Photo Conductivity Frequency Resolved Spectroscopy (PCFRS) [1], directly measures the frequency response of a photoconductive sample or detector under a given light power and photon energy. In this technique, a photoconductive sample is illuminated by photons with energy above the bandgap, and carrying a small amplitude modulation (AM) at a given frequency **f**. The average optical power will create an excess of electron-hole pairs that defines a quasi-static regime, and the superimposed small amplitude modulation is seen as an ac perturbation to this quasi-static regime (small signal treatment).

However, we want to point out that **photons with energy above the bandgap** create electron-hole pairs in both surface and interface space charge regions or near them, wich in turn behave as transverse resistance-capacitance (R-C) systems modulating the effective volume that takes part in the electrical conductivity of the samples [2]. If such samples have a large area to thickness ratio (epitaxial layers), these surface and interface photovoltaic effects dominates. In this way, the frequency response of photoconductive samples shows a kind of R-C behaviour that in PCFRS experiments can be assigned to a non-existing bulk trap and in photodetectors, it produces a low frequency enhanced gain with a kind of Gain-x-Bandwidth product conservation law with incident optical power as we show in this work.

II. THEORETICAL

In PCFRS the excess carrier density is governed by the carrier emission-capture processes, and for small deviations from the quasi-static state, a first order linear differential equation can be written for such evolution. Thus, for sinusoidally modulated light, the sample

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will show a sinusoidal variation in its conductivity, with a given amplitude and phase at each frequency. In the simplest case considered here, where a single lifetime can be defined, the excess carrier density amplitude $\Delta\mathbf{n}$ verifies:

$$\partial\Delta n/\partial t = g - \Delta n/\tau \qquad (1)$$

where τ and **g** are the small signal carrier lifetime and excitation function, respectively. The same rate equation results for the excess carrier in a photoconductive detector under moderate optical excitation (negligible modulation of the majority carrier concentration). For the simplest case of a single recombination lifetime, the solution of the above equation for a sinusoidal modulating frequency ω is well known:

$$\Delta\mathbf{n}(j\omega)/\mathbf{g}(j\omega) = \tau/(1+j\omega\tau) = \tau/(1+\omega^2\tau^2) - j\omega\tau/(1+\omega^2\tau^2) \qquad (2)$$

that states that by monitoring the photoconductive response of the sample in quadrature to a sinusoidally modulated excitation using lock-in detection, a Lorentzian peak is obtained when $\omega\tau=1$. The in-phase component decreases as frequency increases, showing its half-value at this same frequency. The above description of the normalized frequency response is fully equivalent to the well known Bode plot of a first order system, with a cut-off frequency $\mathbf{f_c}=1/2\pi\tau$.

Until now we have considered a bulk sample, without boundary effects, but the sample's free surfaces, and its metal-semiconductor barriers (if any) and interface heterojunctions, will show band-bendings, and consequently carrier depletion (or accumulation) layers. Thus sample conductivity is, in principle, non-homogeneous from the core towards the surfaces or in other words: its conductive core is surrounded by space charge regions whose thickness vary due to the photocarriers that are collected and spatially separated by them. In order to show their behaviour, let us consider the case of a Schottky diode excited by photons with energy above bandgap and with a low index AM illumination, and working in a photovoltaic mode (high load resistance), whose I-V characteristic and small signal circuit model appear in Figure 1.

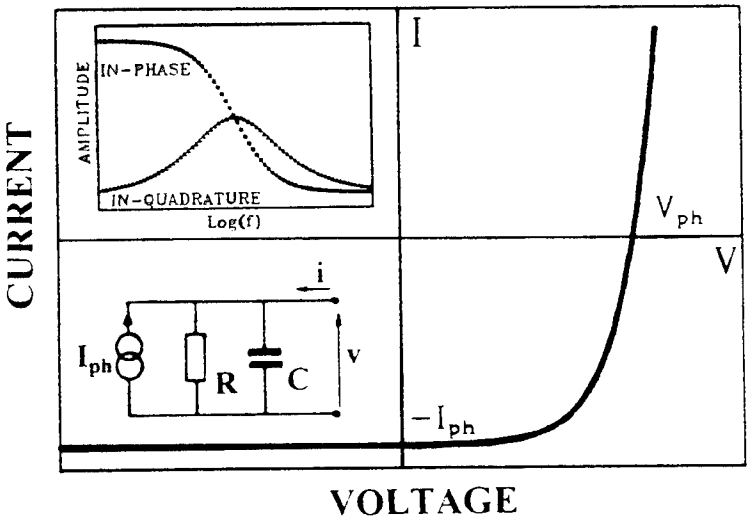

Figure 1. I-V diode (Schottky or junction) characteristic under dc illumination. The inserts in the third and fourth quadrants show its equivalent circuit for ac small signal variations and the components (both in-phase and quadrature) of its photovoltage frequency response to a low index, amplitude modulated light.

Initially the dc optical power creates an internal average photocurrent $\mathbf{I_{ph}}$ that, in turn shrinks the Schottky depletion region in such a way that a dc photovoltage $\mathbf{V_{ph}}$ appears between the diode contacts. Once this $\mathbf{V_{ph}}$ is onset, the optical AM generates small sinusoidal current variations $\mathbf{i=\Delta I_{ph}}$ of $\mathbf{I_{ph}}$, and thus small diode photovoltage variations $\mathbf{v=\Delta V_{ph}}$. The ac photovoltage response (normalized to the ac optical excitation $\mathbf{g(j\omega)}$) is determined by the RC equivalent circuit of the Schottky diode, a parallel complex impedance $\mathbf{Z(j\omega)}$ namely:

$$\mathbf{v(j\omega)/g(j\omega)=\eta Z(j\omega)=\eta R/(1+j\omega RC)=\eta R/(1+\omega^2\beta^2) - j\omega\beta\eta R/(1+\omega^2\beta^2)} \qquad (3)$$

where **j** is the imaginary unit, β is the circuit time constant or **RC** product and η is the light to current conversion efficiency. Equation (3) shows that the in-phase and quadrature components of the ac photovoltage are the same functions that we expected for the PCFRS response (equation 2). Such components are shown in Figure 1. Now the quadrature Lorentzian peaks at the cut-off frequency $\mathbf{f_c=1/2\pi RC}$, **with an amplitude proportional to the diode dynamic resistance R** at the working point ($\mathbf{V_{ph}}$ - $\mathbf{I_{ph}}$). For a Schottky diode whose I-V characteristic is:

$$\mathbf{I = I_{sat}\,(exp(V/nV_t) -1)} \qquad (4)$$

where $\mathbf{V_t}$ is the thermal voltage and **n** is the ideality factor, **R** is:

$$R = \frac{\partial Vph}{\partial Iph} = \frac{nVt}{Iph + Isat} \qquad (5)$$

Equation (5) expresses that under illumination conditions making $\mathbf{I_{ph} >> I_{sat}}$, **R** decreases inversely with the incident power. On the other hand, the depletion capacitance, **C**, changes rather weakly with $\mathbf{I_{ph}}$ (since V_{ph} weakly changes and thence the depletion region width), meaning that the cut-off frequency $\mathbf{f_c}$ of the circuit increases directly with the incident optical power. In other words, the Lorentzian peak of the Schottky photovoltaic response will change its frequency position proportionally to the dc illumination intensity. Hence, the first signature for the small signal photoresponse of a Schottky depletion layer, and by extension for any sample surface depletion region is a linear frequency shift of the imaginary part peak of its small signal photovoltage response under high optical illumination level ($\mathbf{I_{ph} >> I_{sat}}$). As it is well known from capacitance transient techniques, a small space charge voltage drop variation and its corresponding small depletion layer width variation one are linearly related. **Thus, the space charge region width will have a modulation with the same optical power behaviour and cut-off frequency $\mathbf{f_c}$, and the same modulation will appear in the sheet conductivity of a layer having the above space charge region surrounding it.**

In order to study the relative importance of the above surface depletion-layer width modulation effect, let us examine Figure 2, where a cross section of a conductive Hall bar as those used for planar photodetectors is drawn. Let us suppose too that the top surface is covered by a semi-transparent metallic layer creating a Schottky diode. Let us assume that the material is n-type GaAs doped with $\mathbf{N_d}=10^{17}$ cm^{-3}, and we will use a minority carrier lifetime of 10 ns, a value similar or slightly higher than the radiative lifetimes given in [4] for p-type GaAs doped to this level. Finally, and to allow easier comparisons with our samples, let us take the thickness $\mathbf{t}$=1 micron, a surface area of 1 cm^2, and both the width **w** and lenght $\mathbf{L >> t}$.

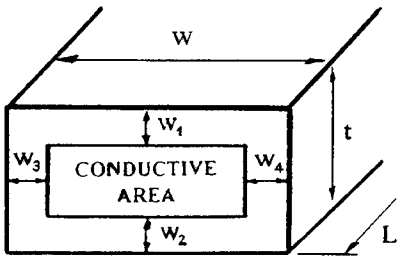

Figure 2. Cross section of a conductive bar showing four peripheral space charge regions associated to four bulk discontinuities.

For blue light illumination we take an absortion coefficient α in GaAs close to 10^5 cm^{-1} [5] and we use to simplify a 100% quantum efficiency. Although the excess hole and electron concentrations should be equal, due to the much higher electron mobility, we can neglect the increase in conductivity due to the excess holes, and consider only the increment due to the electrons. Thus, **to change the sheet resistance of such a sample in 10 parts per million**, we need to create a stationary excess electron concentration of 10^{12} cm^{-3} in our volume (10^{-4} cm^{-3}). This implies to maintain 10^8 minority holes in a region where their lifetime is 10^{-8} seconds, and from equation (1), this requires to generate $10^8/10^{-8}=10^{16}$ electron hole pairs per second. This should be the number of photons crossing our 1 cm^2 semitransparent metallisation.

Under such illumination we have to consider the effect of the space charge edges associated with the sample in figure 2: a) the top metal-GaAs heterojunction (Schottky diode); b) the bottom n-type GaAs/semi-insulating GaAs homojunction and c) the peripheral GaAs/air-surface heterointerfaces. From the conductive area viewpoint, we can neglect the effects related with the two lateral GaAs/air heterointerfaces. To simplify even more the reasoning, we will neglect the influence of the bottom n-GaAs/GaAs substrate homojunction. The 10^{16} electron-hole pairs created per second will contribute to the photocurrent in the upper Schottky diode [5], thus creating a steady photovoltage $\mathbf{V_{ph}}$, since the diode is in photovoltaic mode (no external load). We can evaluate $\mathbf{V_{ph}}$ for an ideal n-GaAs Schottky diode, n=1 in equation (4), using the thermionic theory and a typical barrier height of 0.8 eV [4]. If so one gets a room temperature saturation current of $2.6\text{x}10^{-8}$ A per cm^2. The above 10^{16} generated pairs per second being collected by a metal area of 1 cm^2 produce a photocurrent of $1.6\text{x}10^{-3}$ A, and using equation (4) one gets $\mathbf{V_{ph}}$=0.285 volts. This means that the space charge width $\mathbf{W_1}$ of Figure 2 has to change from its value in the dark (due to the 0.8 eV barrier height) to a new one corresponding to the new barrier height of 0.8eV-0.285eV=0.515eV. This space charge width variation will produce an increase of the conductive area in Figure 2, that in turn will produce a strong conductivity modulation in the sample. For our Schottky diode, we have [4]:

$$W_1 = \sqrt{2\varepsilon\Delta\Phi / qN_d} \qquad (6)$$

where ε is the GaAs dielectric permitivity, $\Delta\Phi$ is the voltage drop and **q** is the electronic charge.

In the dark, using equation (6) with $\Delta\Phi$= 0.8V, we obtain $\mathbf{W_{1dark}}$=0.118 microns, and under illumination $\mathbf{W_{1light}}$=0.095 microns. Thus, the relative variation $\Delta\mathbf{W_1}/(\mathbf{t}-\mathbf{W_1})$ of the conductive thickness is: (0.118-0.095)/(1-0.118)= 0.026. This modulation of $\mathbf{W_1}$ produces an increase (2.6%) of the conduction cross area in Figure 2, and therefore modulates the sheet conductivity of the sample, by a factor that is **2600 times greater than the intended 10 ppm variation due to the carrier concentration variation**. The conclusion is clear: **the**

photoconductive effect just due to the bulk photocarrier concentration modulation will be completely masked by the photovoltaic transverse area modulation effect. This result obtained for the dc modulation can be easily applied for the ac one.

Although this effect has been discussed for the upper Schottky diode, it can be extended to the bottom junction where a band bending exists. In a general case, each space charge region will behave as a Schottky diode with its own dynamic resistance, and they will give some ghost peaks in PCFRS experiments or in the frequency response of photoconductive detectors. This is so because the conductivity of the sample in Figure 2 is directly proportional (although opposite in sign) to any $\mathbf{W_1}$ variation ($\Delta \mathbf{W_1}$) and in turn this is proportional to any small induced photovoltage $\mathbf{v} = \Delta \mathbf{V_{ph}}$ as it can be shown by derivating equation (6). If so, one gets:

$$\Delta W_1 = - (W_1/2\Delta\Phi) \times \Delta v_{ph} \qquad (7)$$

where the term $\Delta\Phi$ is the net voltage drop, equal to the built-in voltage minus the dc induced photovoltage $\mathbf{V_{ph}}$. From equation (7) and the previous comment, we can say that **the sample conductivity is linearly modulated by the transverse space charge region reactions due to the induced photovoltages and evenmore, this modulation is dominant.**

III. EXPERIMENTAL

To verify the above analysis, Hall bars were fabricated on a 1 micron thick GaAs layer grown by MBE onto a semi-insulating GaAs substrate. The doping level was 10^{17} cm^{-3} and the bar dimensions are 100x700 microns. On the top of some of the bars, a semitransparent Ti metallisation gate was deposited, while the remaining ones have a "naked" GaAs-air surface. Standard Hall measurements performed on these "naked" samples gave a $0.85x10^{17}$ cm^{-3} free electron concentration. The I_V Schottky diode characteristics were measured at 295K using the gate as anode and the two current injecting pads at the ends of the sample as the cathode, in order to reduce series access resistance. An ideality factor n=1.14 and a barrier height of 700 meV were deduced. Capacitance-Voltage measurements taken at 10 KHz, to reduce any series resistance effect, gave $N_d=0.91x10^{17}$ cm^{-3} net donor concentration and 0.7 V as built-in voltage, thus confirming the above barrier height.

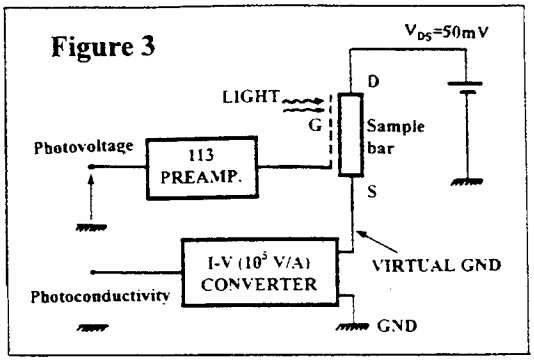

Figure 3

Figure 3 shows the experimental set-up used to perform the photovoltage and photoconductivity measurements. The GaAs Hall bars with semitransparent gates are actually fat FET transistors, although we used them as simple photoconductive bars with the added possibility of checking the photoinduced voltage at the gate, and its frequency evolution.For floating gate measurements, the gate is loaded by the input impedance (1 GΩ shunted by 15 pF) of the preamplifier (an EGG-PAR 113 model powered by batteries) used to monitor the photovoltage.

Photoconductivity measurements with and without the preamplifier connected to the gate were performed, and we checked that the same results were obtained if one added a 15 pF capacitor connected between gate and ground.

IV. RESULTS AND DISCUSSION

The photovoltage frequency response generated at the semi-transparent gate in one of the GaAs Hall bar samples at T=299K is shown in Figure 4-a. Two kinds of illumination were used: an AlGaAs/GaAs red LED (λ=0.65 μm) driven by 10 mA dc current with a 10 % AM, and a GaN blue LED (λ=0.45 μm) driven by 1 mA dc current with a 12 % AM. A dc photovoltage $\mathbf{V_{ph}}$=120 mV at the Schottky diode, for both light sources was obtained. Both the real and imaginary parts of the ac photovoltage are shown in Figure 4-a, where one can see that for the blue photons the response is about a 20 % higher than for the red LED, in agreement with the 12 vs 10 % AM indexes used. It is clear in both cases that the imaginary parts peak at 300 Hz, thus reflecting that the Schottky dynamic resistance is the same in both cases, since the parasitic capacitance **C** due to the Schottky diode itself and to the cryostat inner and outer coaxial wires also is the same in both cases. The ac photovoltage signals are of the order of 3 mV_{peak}.

The photoconductivity signals obtained under the same conditions of those of Figure 4-a are shown in Figure 4-b. In this case, the imaginary parts peak close to 300 Hz, but not exactly at this frequency. Evenmore, it peaks at about 200 Hz for the blue case and at about 350 Hz for the red illumination. If only the top Schottky space charge modulation was responsible for the above photoconductivity response, one would expect the same PCFRS peak frequency for both blue and red photons. However, one micron below the Schottky barrier, we have the n-GaAs/GaAs space charge region (bottom junction) that also reacts if photons are absorbed near it.

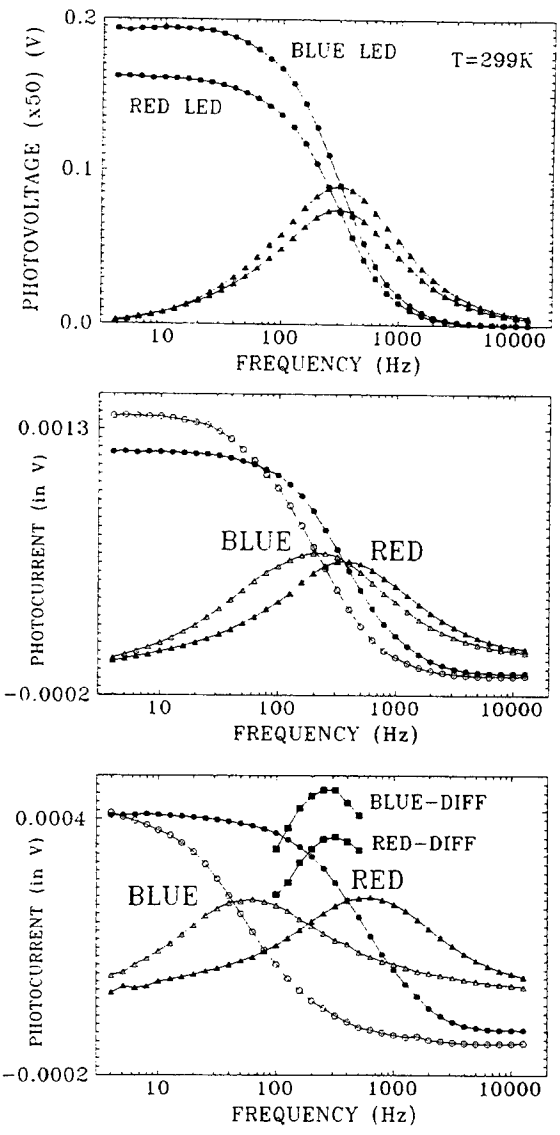

Figure 4. a) Photovoltage signals at the semitransparent gate under the two light sources described in the text. b) and c) Corresponding photocurrent signals (see text).

To separate both contributions, if the gate is connected to ground and the photoconductivity is measured again, only the contribution of the epitaxial to substrate homojunction will be obtained. These measurements are presented in Figure 4-c. In this case and for the red light, the PCFRS imaginary part peaks above 600 Hz, while for the blue light the PCFRS imaginary part peaks near 60 Hz. The reason for the above behaviour is that the blue light is absorbed near the surface, while the red one easily crosses the whole 1 micron layer. As we said in the previous section, if few photons are absorbed at the bottom junction, a low photocurrent is generated or a low photovoltage is created there. This means that the dynamic junction diode resistance is high and thus the cut-off frequency $\mathbf{f_c}$ is correspondingly low, while the ac photovoltage response and its associated conductive area modulation both are high. This explains the, at first sight puzzling result, concerning the fact that amplitudes are similar in Figure 4-c, although a much lower photon flux is expected to reach the bottom junction in the blue case.

The conductivity modulation appearing in our GaAs Hall bar samples is about 5.6×10^{-4} its value at room temperature (2.35 KΩ). A final check of the above statements has been done by sustracting point by point the Lorentzian peaks of Figures 4-b and 4-c. If so, two new conductivity Lorentzian peaks are obtained, (see curves labelled as BLUE-DIFF and RED-DIFF in Figure 4-c) both centered at 300 Hz, as it corresponds to the upper Schottky transverse photovoltaic reaction with $\mathbf{f_c}$=300 Hz. In this way, both the upper Schottky space-charge modulation effect and the bottom GaAs-substrate homojunction one are clearly shown, as well as their influence in the photoconductive response of the samples.

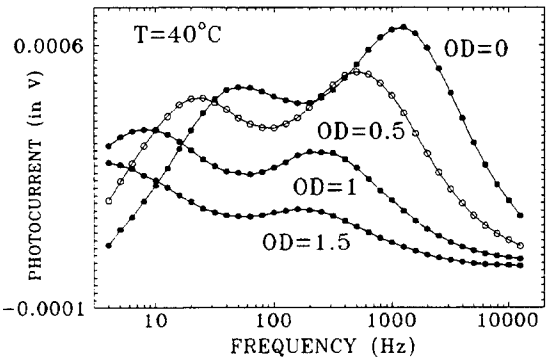

Figure 5. PCFRS spectra obtained at T=40°C for a "naked" GaAs bar under four optical powers : P, $10^{-1/2}$ times P, P/10 and $10^{-3/2}$ times P, of the blue light described in the text.

Figure 5 shows the photovoltaic response of a "naked" photoconductive Hall bar to the same blue light with 10 % AM index modulation. Four optical powers were used by means of optical filters with different optical densities (OD). The foreseen $\mathbf{f_c}$ shift with optical power is clearly seen as well as the two peaks corresponding to the upper (surface) and bottom (epilayer to substrate) space charge regions. Further discussions and conclusions are given in [2].

V. CONCLUSIONS AND FURTHER APPLICATIONS

We have shown that the small signal frequency response of epitaxial photoconductive detectors is determined by the surface and interface transverse space-charge reactions due to photovoltages induced there by the photons. Although very high photoconductive gains can be achieved under this mechanism, low cut-off frequencies due to the R-C behaviour are expected. Only at very high optical powers, such band-bendings will be flatten, and the cut-off frequency will be determined by the effective recombination lifetime of the electron-hole pairs in the detector bulk (standard photoconductive effect). Figure 6 summarizes this behaviour.

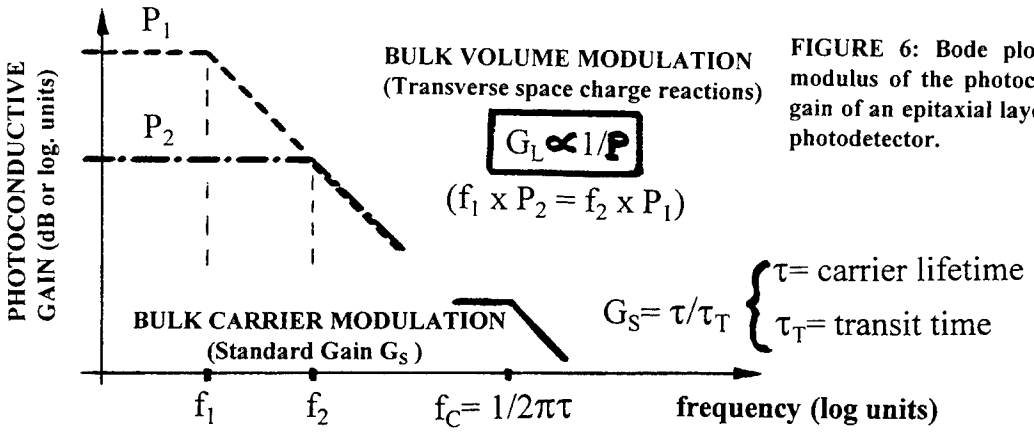

FIGURE 6: Bode plot for the modulus of the photoconductive gain of an epitaxial layer used as photodetector.

From the above considerations, the gain of photoconductive detectors can be increased by means of intentionally added space-charge regions parallel to the surface. One possibility is a set of δ–doping layers embedded in the otherwise bulk region. However, III-V materials grown onto substrates oriented along non-standard indexes as [111] offer two clear advantages due to the piezoelectric (PE) fields that can be obtained in strained layers. The first one is the high degree of control of such PE fields by means of the alloy composition of the layers. The second one is due to the "fine grain" structure (at an atomic level) of such PE fields as compared to the electric ones associated to ionized impurities, thus preventing impurity scattering and enhancing both mobility and standard gain (lifetime to transit time ratio [5]) in the photodetector.

When frequency-domain techniques as PCFRS, or time-domain ones as Photo Induced Current Transient Spectroscopy (PICTS) are used in epitaxial conductive layers, the transverse space-charge reactions should be considered for photons with energy above bandgap. In this context , the "simple" measurement of the photoconductive gain in epitaxial layers of wide-gap materials as GaN, can present difficulties due to the large signal character of the chopped light used associated to a lock-in detection technique. In such materials, very high band-bendings can exits, thus giving rise to strongly non-exponential time decays due to the high photovoltage swings that can take place. Since the dynamic resistance R exponentially depends on the photovoltage, the chopping frequency has to be selected properly or, at least, checked with the cuasi-dc results. As an example, the gain dependence with power (P) of a GaN photoconductive sample at 300 K, using an He-Cd UV laser chopped at 18 Hz, was found proportional to $P^{-0.6}$. Nevertheless, using ON-OFF periods of several minutes, it was found proportional to $P^{-0.9}$, quite close to the P^{-1} law shown in Figure 6, a fact we are trying to explain at present.

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Two-dimensional all-optical parallel-to series TDM and demultiplexing by spectral-holographic methods

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Abstract

A two-dimensional all optical processor which multiplexes a rectangular array of parallel incoming signals into a series output transmitted through a single optical fiber is suggested for the first time along with a corresponding 2-dimensional series to parallel transformer. The system uses four-wave interaction in a hologram, both for MUX and deMUX. It can be used for the direct fiber-optical transmission of many time-dependent images, without going through the usual video serialization, as well as for multiple analog or digital, video and audio-transmissions, or multiplexing and demultiplexing of any nature.

All-optical one-dimensional parallel-to serial conversion by holographic one-dimensional space-to time frequency encoding was recently introduced [1], along with the previously known series-to-parallel transformation. However, the large discrepancy between the Gbit/s capacity of coaxial cables and the Tbit/s rates achievable in optical fibers for photonic networks, requires the multiplexing of roughly 10^3 incoming conventional signals in a single optical fiber. This requires harnessing of the full power of Fourier-optical holographic methods, by using both dimensions of optical wavefronts for data processing. The processor system we propose consists of two independent optical channels C_t and C_s for carrying temporal signals and spatial information, both in its parallel-to-series (Fig. 1) and in its series-to-parallel (Fig. 2) parts. C_t is shown with continuous lines, representing ultra-short pulsed beams, while C_s is shown with dotted rays, using longer pulses.

C_t passes the ultra-short pulse wave-fronts through a blazed 2-dimensional reflecting diffraction grating G_1 which is described below, followed by a lens L_1 of focal length F, a real-time hologram H in its focal plane, an identical lens L_2, and a second, similar, 2-D reflection grating G_2, with a distance F between each of these 5 elements on their common optical axis.

C_s is an optical Fourier transform channel which inputs the modified image of a rectangular array of sources. C_s introduces this image through the semi-transparent mirror M together with a reference beam. They are introduced backwards through the lens L_2, creating a Fourier-transform hologram H which in turn acts on the forward-propagating C_t beam, splitting it up in a number of temporally displaced beams equal with the number of sources present in the input of C_s. The sum of these beams is Fourier-transformed back to the time-domain, yielding the desired *serial output* of the given parallel data input. The modification hikes line intervals n times.

This paper brings first the analysis of the parallel-to-series convertor, and then a brief discussion of the corresponding receiver. The multiplexer works in two steps.

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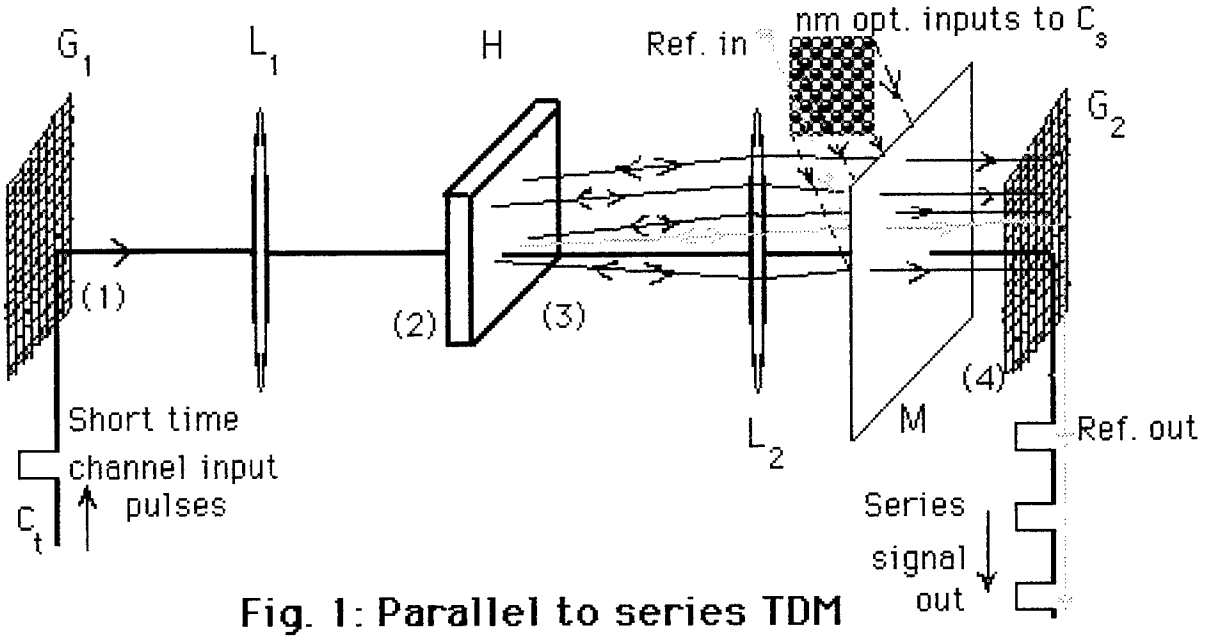

Fig. 1: Parallel to series TDM

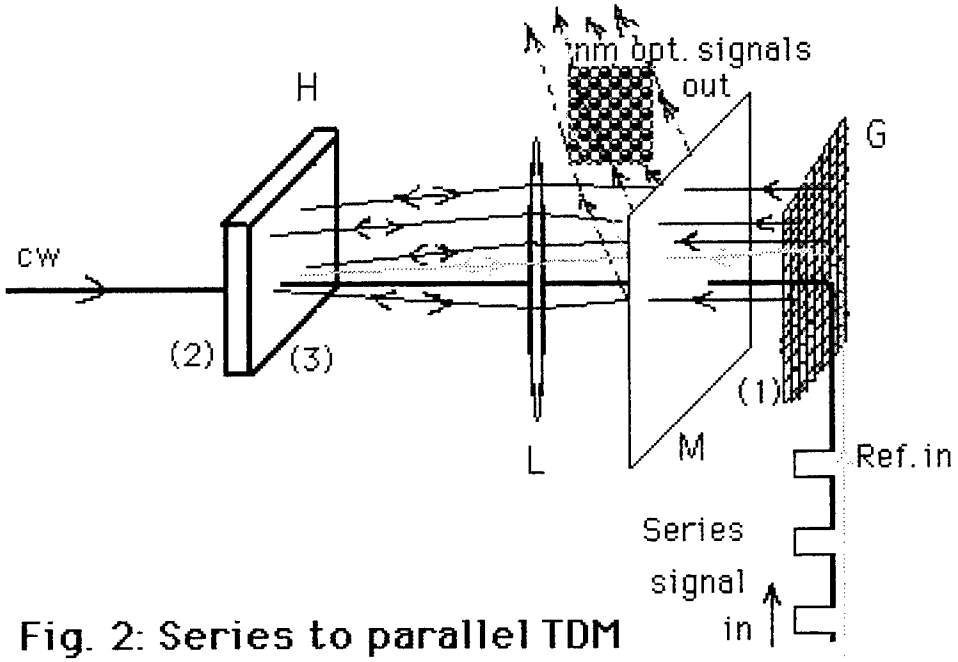

Fig. 2: Series to parallel TDM

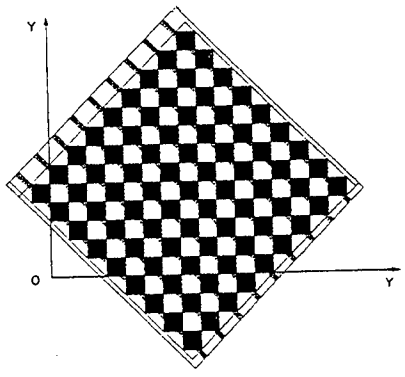

Fig. 3: Two-dimensional diffraction grating, diagonally blazed.

1) In a first step, starting from a single mode-locked laser, a 2-dimensional manifold of N=n×m coherent beams is created by multiple beam-splitting, along with a reference beam. By synchronized sampling and birefringent synchronous modulation, we transfer the information from each one of the N incoming coaxial cables to one of the N beams, in the form of pulses of length τ. The reference beam always carries the standard, unmodulated pulse generated by the laser. Part of the reference beam is separated by a beam splitter and is then re-shaped [2,3] for C_t to be ultrashort of duration τ_o ($<<\tau$, up to $10^{-3}\,\tau$, of the order of the reciprocal carrier bandwidth, a few tens of femtoseconds). The rest of the reference beam separated by the beam splitter goes to the C_s channel together with the N modulated beams. The first step thus creates *a rectangular array of luminous sources with n columns and m rows plus the reference beam, which yield the (τ) input beam to C_s,and an ultrashort sequence of pulses which yields the (τ_o) input beam to C_t*. The input to C_t is thus a regular sequence of pulses in time, of the form

$$s(t) = p(t-t_o)\exp(j\omega_c t), \tag{1}$$

with Fourier transform

$$P(\omega-\omega_c)\exp[-j(\omega-\omega_c)t_o], \tag{2}$$

where $P(\omega)$ is the Fourier transform of $p(t)$.

2) In the second step, this input beam passes through C_t. Let the temporal transfer function of C_t be $H(\omega)$. Then the output spectrum will be

$$H(\omega)P(\omega-\omega_c)\exp[-j(\omega-\omega_c)t_o]. \tag{3}$$

To calculate $H(\omega)$, we calculate the output resulting from the passage of a monochromatic input $\exp[j(\omega t-\mathbf{kr})$ through C_t. Let **k** be incident on the 2-D diffraction grating located in the xy plane with directing cosines α and β to the x and y axes. The blazed 2-D diffraction grating is obtained by applying a squared lattice chess board-like black deposit on a 1-D blazed diffraction grating at 45° to the diffraction grating, i.e., so that the x and y axes of the applied chess board are at 45° from the groves of the 1-D blazed grating (Fig. 3). The lattice constant of the applied chess-board lattice is twice the side of any white or black field on the chess board, and equals the constant of the original blazed lattice times $2^{1/2}$. The diffracted optical field (Fig. 1) generated by the monochromatic input right after the plane P_1 of the grating is

$$s_1(x,y;\omega) = \exp[-j(\omega-\omega_c)(\alpha x+\beta y)/c]\, w(x,y), \tag{4}$$

where w(x,y) is the pupil function of the grating. After passage through the lens L_1 the optical field in plane P_2 right before the hologram is the Fourier transform of the field in Eq. (4), given by

$$s_2(\xi,\eta;\omega) = W[\xi+\alpha(\omega-\omega_c)/2\pi c, \eta+\beta(\omega-\omega_c)/2\pi c], \quad (5)$$

where $W(\xi,\eta)$ is the spatial Fourier transform of $w(x,y)$. The wave numbers ξ and η are expressed in terms of the spatial Cartesian coordinates X and Y in P_2 by $\xi=\omega X/2\pi cF$ and $\eta=\omega Y/2\pi cF$. We note parenthetically that, as indicated by Eq. (5), an optical pulse introduced into the system will have its various Fourier components spatially dispersed along the diagonal of the Fourier transform plane, each occupying an area determined by the function $W(\xi,\eta)$.

We now take into account that a spatial Fourier transform hologram of the above-mentioned rectangular n×m input array has been independently recorded by C_s in the hologram H of Fig. 1. This hologram is a superposition of the n×m holograms of the individual luminous sources present in the rectangular input array, with amplitudes $A_{\mu\nu}$ corresponding to the bit of information carried by the channel $\mu\nu$ to be multiplexed. This hologram serves as a temporal frequency filter with transmittance

$$t(\xi,\eta) = \sum_{\mu=1}^{m}\sum_{\nu=1}^{n} A_{\mu,\nu}\exp[j2\pi(\omega_w/\omega)(\nu\Delta_x\xi+\mu\Delta_y\eta)], \quad (6)$$

where Δ_x is the geometrical distance between columns and Δ_y is the modified distance between the rows in the regular input array fed into C_s, whereas ω_w is the frequency of the writing field used for recording the hologram, in our case ω_c. It is necessary to take $\Delta_y \geq n\Delta_x$, and suitable to choose, e.g., $\Delta_y = (n+1)\Delta_x$. This is achieved with the help of a convergent cylindrical magnifying lens placed in front of the rectangular array of light sources, with its cylindrical axis parallel to the x-axis, which would cause the separation between rows to appear larger. In addition, we assume $(n+1)m\Delta_x+c\tau_0 \leq c\tau$.

Returning now to C_t, right after passage through the hologram, the optical field in P_3 will be

$$s_3(\xi,\eta;\omega) = s_2(\xi,\eta;\omega)\, t(\xi,\eta). \quad (7)$$

After passage through L_2, the field in plane P_4 is given by a second spatial Fourier transform which yields

$$s_4(x,y;\omega) = \sum_{\mu=1}^{m}\sum_{\nu=1}^{n} A_{\mu,\nu} w[-x+\nu\Delta_x, -y+\mu\Delta_y] \times\exp[(j/c)(\omega-\omega_c)[\alpha(x-\nu\Delta_x(\omega_w/\omega)) + \beta(y-\mu\Delta_y(\omega_w/\omega))]. \quad (8)$$

This field is diffracted by the 2-D grating G_2 and yields the output field propagating in the k" or z" direction

$$s_5(x",y";\omega) = \sum_{\mu=1}^{m}\sum_{\nu=1}^{n} A_{\mu,\nu} w[-x"+\alpha"\nu\Delta_x, -y"+\beta"\mu\Delta_y]$$

$$\times\exp[(j/c)(\omega-\omega_c)(\omega_w/\omega)(\alpha\nu\Delta_x + \beta\mu\Delta_y)] \equiv H(\omega). \qquad (9)$$

This is the temporal transfer function of the system. Here α" and β" are directing cosines of the outgoing wave vector **k**". Assuming $\Delta_y = (n+1)\Delta$ and $\Delta=\Delta_x$,

$$H(\omega) = \sum_{\mu=1}^{m}\sum_{\nu=1}^{n} A_{\mu,\nu} w[-x"+\alpha"\nu\Delta_x, -y"+\beta"\mu\Delta_y]$$
$$\times\exp\{j(\Delta/c)(\omega-\omega_c)(\omega_w/\omega)[\alpha\nu + \beta\mu(n+1)]\} \qquad (10)$$

The temporal output function allows the determination of the serial output of the multiplexer as the Fourier transform of Eq. (3)

$$s_o(x",y"; t) = [\sum_{\mu=1}^{m}\sum_{\nu=1}^{n} A_{\mu,\nu} w[-x"+\alpha"\nu\Delta_x, -y"+\beta"\mu\Delta_y] p(t-t_o-r\delta t)] \exp(j\omega_c t). \quad (11)$$

Here $r = \nu + \mu(\beta\Delta_y/\alpha\Delta_x) = \nu + \mu(\beta/\alpha)(n+1)$; for $\alpha=\beta$, $r = \nu + \mu(n+1)$. The interval δt was defined as $\alpha\Delta_x$.

Eq. (11) shows that the parallel-to-series or multiplexing operation was performed. Along with the series signal, the non-diffracted portion of the readout beam coming from the hologram H in Fig. 1 is also transmitted to the receiver as a reference signal.

In principle, all beams could be reversed. This observation makes the description and operation of the demultiplexer shown in Fig. 2 straightforward. A hologram is recorded at the receiver site between the incoming serial signal shown by Eq. (11) and the received reference signal, both having first been diffracted in reflection by the identical diffraction grating G. This real time hologram is modulating the cw monochromatic readout wave front coming from the left in Fig. 2 and passing through the hologram, thereby creating $N=n\times m$ beams. The result is thus a two-dimensional $n\times m$ parallel optical output which is extracted with the help of the semi-transparent mirror M and projected on a $n\times m$ array of outgoing optical fibers, or on a similar array of photodetectors.

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EFFECT OF THE FREE CARRIER CONCENTRATION ON THE ESCAPE TIME OF EXCITONS IN QUANTUM DEVICES

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We have studied the effect of the electronic many-body interaction and of an external field on the tunneling escape rate in double barrier devices. Lifetimes of photoexcited excitons in quantum wells have been obtained at different carrier sheet densities by solving selfconsistently the time dependent Schrödinger and Poisson equations. Results showed that the excitonic escape time is strongly affected by the area free carrier density in the quantum well.

Since its discovery by Tsu and Esaki [1], resonant tunneling through semiconductor structures has been the object of a great attention due to its possible applications to ultra-high speed electronic devices [2]. With the development of such devices, it has become important to carry out theoretical and experimental studies on the tunneling process of carriers. One of the most important time-domain experiments in the case of double barrier heterostructures was realized by Tsuchiya *et al.* [3]. They studied the decay of an exciton localized between two barriers in a single quantum well using a technique of picosecond time-resolved photoluminescence.

Taking into account such an experiment, and from a theoretical poit of view, it has been recently shown that an excitonic wave function will be needed to explain the carrier wavepacket dynamics in the case of large applied electric fields [4]. In addition to this, the electron-phonon coupling has also been studied finding that the different phonon modes can contribute significantly to the carrier tunneling escape process [5].

From an experimental poit of view, charge accumulation effects in a double barrier structure has been experimentally studied [6] using photoluminescence and photoluminescence-excitation spectroscopy. In this way, Yoshimura *et al.* [6] found that many-body interactions can play an important role in the Stark effect for such a double barrier system. However, one remaining key question in the theoretical study of the tunneling escape process is the analysis of many-body effects in the quantum well region. We know that if a large number of electrons are photoexcited in a quantum well, the electrical properties can be strongly modified due to charge-buildup effects. In the last years, many-body interactions in semiconductor quantum wells have been studied with the using of a nonlinear Schrödinger equation [7] finding chaotic behavior in the tunneling transport through a double barrier structure. Taking into account this, in this work we will study the time-dependent evolution of an excitonic wave packet in the double barrier structure considering many-body interactions. The method of calculation will be based on the discretization of space and time for the carrier wave functions. We will show that carrier lifetimes can be strongly modified due to many-body interactions.

In order to study the dynamics of tunneling, we need to solve the time-dependent Schrödinger equation associated with the Hamiltonian for a spinless exciton in the heterostructure region. The excitonic wave function will be given by two nonlinear Schrödinger equations [4,5]

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$$i\hbar\frac{\partial}{\partial t}\psi_{i,j}(z_{i,j},t)=\left[-\frac{\hbar^2}{2m^*_{i,j}}\frac{\partial^2}{\partial z^2_{i,j}}+V_{i,j}(z_{i,j})+W_{i,j}+eFz_{i,j}\right]\psi_{i,j}(z_{i,j},t) \quad (1)$$

being $i=e, j=h$.

Both equations have to be solved together since, in the mean field aproximation, the term

$$W_{i,j}(z_{i,j})=\frac{4\pi e^2}{\varepsilon_0}N_{i,j}\int_0^z(z'-z)(\psi^2_{i,j}-\psi^2_{j,i})dz \quad (2)$$

couples ψ_e and ψ_h. The subscripts i,j refer to electrons or holes, respectively, and V_e (z_e), V_h (z_h) are the quantum well potentials. The m^*_e and m^*_h values are the effective masses. The F term is an external applied electric field, and $W_{i,j}$ is the potential given by the carrier-carrier interaction in the heterostructure region. Such a many-body potential is given by the Poisson's equation

$$\nabla^2 W_{i,j}(z)=-\frac{4\pi e^2}{\varepsilon_0}N_{i,j}\left|\psi_{i,j}(z)\right|^2 \quad (3)$$

where ε is the GaAs dielectric constant and $N_{i,j}$ is the initial electronic (hole) sheet density.

Now we discretize time by a superscript n and spatial position by a subscript j and k for the conduction and valence band, respectively. Thus, $\psi_e \rightarrow \kappa^n_j$ and $\psi_h \rightarrow \varphi^n_k$. The various $z_{e,h}$ values become $j\delta z$ and $k\delta z$ in the conduction and valence band, where δz is the mesh width. Similarly, the time variable takes the values $n\delta t$, where δt is the time step. In this way, and to treat the time development, we have used an unitary propagation scheme for the evolution operator in both conduction and valence bands obtaining a tridiagonal linear system that is solved by standard numerical methods [4,5]. In Ref. 7 the authors have solved the nonlinear Schrödinger equation using a many-body potential proportional to the charge density inside the double barrier. This approximation is not valid for our tunneling sytem. In our case, the electron-electron interaction takes place for all z values, i.e., we have assumed the existence of an uniform positive background of charge density in the GaAs double barrier electrodes. Taken into account this, we have also solved the Poisson's equation associated with $W_{i,j}$ using an standard tridiagonal numerical method for each t value.

In our calculations, we have assumed that an electron-hole pair is initially created in the center quantum well at $t=0$. Then, Eqs. (1), (2) and (3) are numerically solved using a spatial mesh size of 0.5 Å and a time mesh size of 1fs and a finite box (2000 Å) large enough as to neglect border effects. We have considered a GaAs/$Ga_{0.75}$ $Al_{0.25}$ As double barrier structure which consists of a 100 Å-wide GaAs quantum well and two $Ga_{0.75}$ $Al_{0.25}$ As barriers of 15 Å-thickness.

The numerical integration in time allows us to obtain the carrier charge density, $Q_{a,b}$, in a defined semi-conductor region $[a,b]$ at any time t,

$$Q_{a,b}(t)=\int_a^b dz\left|\psi(z,t)\right|^2 \quad (4)$$

where $[a,b]$ are the quantum well limits. So that, the decay of the integrated electron charge density, initially trapped in the quantum well, follows essentially the exponential law [4,5],

$$Q_{a,b}(t)=Q_0\exp(-t/\tau) \quad (5)$$

where τ is the electron lifetime and Q_0 is a constant. Through the numerical integration of Eqs. (1), (2) and (3), and using Eq. (5), it is possible to obtain the electron and hole lifetimes at different applied electric fields.

In Figures 1-2, we have plotted the electron charge density at different N_i values.

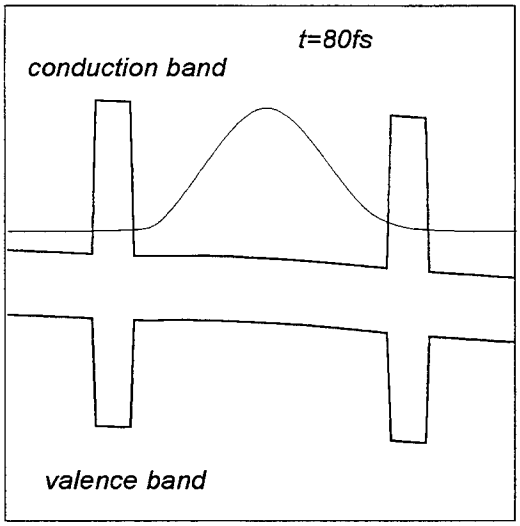

FIG. 1. Electron charge density in our double barrier structure potential at t=80 fs. The applied electric field is F= 10 kV/cm. The initial two-dimensional sheet density is N_i =0.4×10^{11} cm^{-2}.

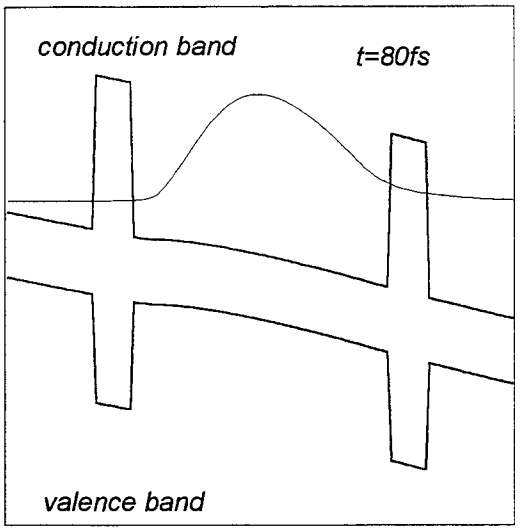

FIG. 2. Electron charge density in our double barrier structure potential at t=80 fs. The applied electric field is F= 10 kV/cm. The initial two-dimensional sheet density is N_i =2.0×10^{11} cm^{-2}.

In Figures 3-4, we have also plotted the different carrier lifetimes versus N_i at different electric field values. It is clearly shown that lifetimes are decreased as we increase the electric field. Such an effect is due to the field-induced tunneling escape process of the electron-hole pair confined in the quantum well region.

The electron will escape to the right electrode due to its negative charge and, simultaneously, the hole will escape to the left electrode due to its possitive sign in the electric charge. In addition, we can also notice that the hole lifetimes (Fig. 4) are higher than electron lifetimes (Fig. 3). This can be easily explained taking into account that the field-induced tunneling in the valence band is difficult due to the higher hole effective-mass.

In Figures 3 and 4 we can notice that the carrier lifetimes are exponentially decreased as we increase the carrier sheet density N_i . Such an effect is due to the filling up of the quantum well because of the initial wave packet form. Increasing N_i , the initial filling up of the quantum well potential will be also increased due to charge build-up effects. It is clearly shown in Figures 3 and 4 that carrier lifetimes can be modified several orders of magnitude by charge accumulation phenomena. We know that we can obtain only a 10-20% higher electron and hole lifetime values by excitonic effects [4]. In addition and by the presence of phonons in the double barrier, τ values are also slightly modified [5]. So that, we can notice that charge accumulation effects can play a decisive role in the study of excitonic tunneling escape process in double barriers.

In this way, many-body effects in double barriers should be taken into account to explain

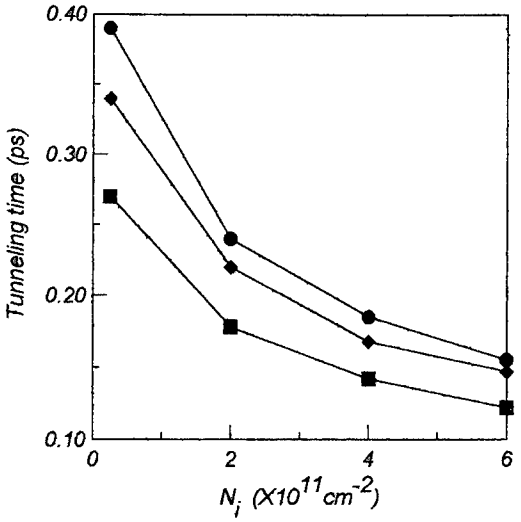

FIG. 3. Electron lifetimes vs N_i at different applied electric fields. Circles: F=1 kV/cm. Diamonds: F=5 kV/cm. Squares: F=10 kV/cm.

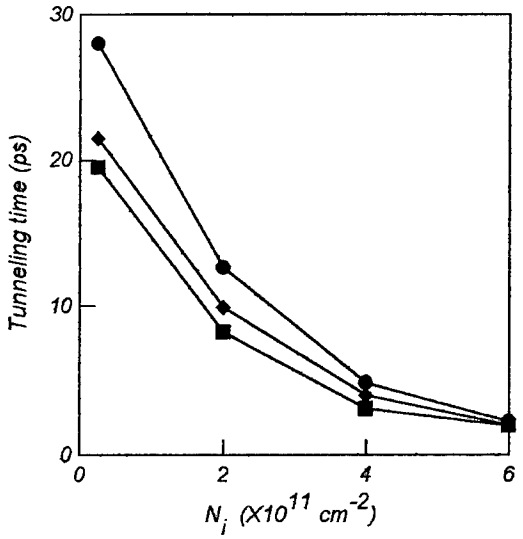

FIG. 4. Hole lifetimes vs N_i at different applied electric fields. Circles: F=1 kV/cm. Diamonds: F=5 kV/cm. Squares: F=10 kV/cm.

differences between theoretical and experimental tunneling times [3-5]. We should also remark that in our numerical evolution we have obtained that if N_i is large enough we can neglect the Coulomb interaction effects in Eq. (1), i.e., $W(z) \sim 0$. Such a result is in agreement with available experimental data. Yoshimura *et al.* [6] found that as carriers accumulate, excitonic states get unstable and recombination process gets dominated by the free-carrier process.

In summary, in this work we have numerically integrated in space and time the effective-mass nonlinear Schrödinger equation for an electron-hole pair in a double barrier structure considering many-body interactions. It is found that charge accumutation effects in both valence and conduction bands can play an important role in the excitonic tunneling process. From a practical point of view, the study of such an effect can be fundamental to understanding the carrier dynamics across double barriers, and thus, the operating principles of Stark-effect-based semiconductor devices.

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TERAHERTZ EMISSION FROM DIRECT CREATED EXCITONS IN QUANTUM WELLS

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We have studied the dipole electromagnetic radiation emerging from electrically pumped excitons tunneling between asymmetric double quantum wells, and taking into account the two-particle nature of the process. Transition between direct and indirect excitons affects the charge oscillation of direct created excitons and so, the terahertz emission. The frequency of this process is one order of magnitude higher than the photoexcited exciton emission.

Recently, GaAs/GaAlAs semiconductor coupled quantum wells have been used to observe tunneling charge oscillation in solids [1]. In such an experiment, the superposition of both symmetric and antisymmetric quantum well eigenstates in the conduction band led to coherent tunneling between both quantum wells, and thus, to an electron-hole pair with a time-dependent distance. In this way, a time-varying excitonic dipole moment in the wells was obtained, so that it allowed the emission of electromagnetic radiation at the oscillation frequency .

There is also a great interest in other related phenomena as spatially coherent quantum well (QW) excitons, with an in-plane momentum $\mathbf{k}_{ex||}\sim 0$, due to their capability of radiating in the perpendicular direction to the QW. To the present, resonant optical pumping was needed to create efficiently such excitons. In a recent experiment and theory, Cao et al. [2] have shown the possibility of the direct creation of $\mathbf{k}_{ex||}\sim 0$ electrically pumped QW excitons. It seems interesting to extend the analysis to asymmetric coupled quantum wells (ACQW) . In the direct generation of excitons electrons tunnel from a n-type material through a barrier to the left quantum well (LQW). Because of the structure is closed by a p-type material, the process is assisted by the electron-hole Coulomb interaction, obtaining a two-particle process. We assume that holes thermally diffuse into the right quantum well (RQW). Under resonant conditions between two adjacent wells with different widths, electron-in-excitons can tunnel back and forth from one well to the other. So that, we can expect that the generated time-dependent dipole can radiate THz electromagnetic waves before radiative recombination. The process is widely explained in reference [3].

The problem we are concerned in is the dynamical evolution of excitonic electron-hole pairs [4] in ADQW. The method of calculation is based on the discretization of space and time for the carrier wave functions. The injected-free electron, localized initially in the n-doped material is simulated by a Gaussian wave packet. After crossing the first barrier, the electron is trapped by the Coulomb interaction and forms the cross exciton with the hole. Under resonant conditions the electron-in-exciton packet is a linear superposition of the two eigenstates in the conduction band, and hence, non-stationary. Subsequently the electron-in-exciton packet will oscillate between the left and right wells. Meanwhile, the hole packet will remain localized in the right well. Besides this, we have two different exciton binding energies [5,6] that affect the wave packet dynamics.

We will consider in this work the ACQW potential represented in Fig. 1. The left electrode is

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a n-doped $In_{0.53}Ga_{0.47}As$ layer. A 100 Å $In_{0.52}$ $Al_{0.48}As$ layer separates the electrode and the left QW. The left (80Å) and right (60 Å) wells consist of $In_{0.53}Ga_{0.47}As$. The barrier between the wells consists of a 30 Å wide $In_{0.52}$ $Al_{0.48}As$ layer. The right electrode is a p-doped $In_{0.52}$ $Al_{0.48}As$ layer. We have chosen a right quantum well width that allows electron-in-exciton coherent tunneling between the wells in the conduction band at the same applied field that is required for the free electron resonance from the n-doped electrode to the electron-in-exciton state in the left well. We have assumed a $m_e^* = 0.042m_0$ effective mass in the conduction band and a $m_h^* = 0.5m_0$ heavy-hole mass. In order to study the dynamics of tunneling, we need to solve the time-dependent Schrödinger equation associated with the Hamiltonian for a spinless exciton in the heterostructure region. The excitonic wave function Φ is given by

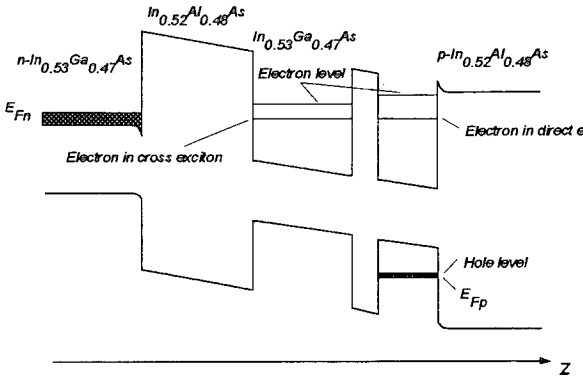

Figure 1. Asymmetric double quantum well under electron-in-exciton resonant condition.

$$\Lambda\Phi(r_e, r_h) = i\hbar\frac{\partial}{\partial t}\Phi(r_e, r_h) \tag{1}$$

where we have

$$\Lambda(r_e, r_h) = \Delta(r_e, r_h) + \sum_{i=e,h}\left[-\frac{\hbar^2}{2m_i^*}\frac{\partial^2}{\partial z_i^2} + V_i(z_i)\right] \tag{2}$$

and the operator Δ

$$\Delta(r_e, r_h) = -\frac{\hbar^2}{2\mu_{xy}}\nabla_{xy}^2 + V_C(\rho, z_e - z_h) \tag{3}$$

where the subscripts e,h refer to electrons or holes, respectively, and $V_e(z_e)$, $V_h(z_h)$, are the quantum well potentials. The m_e^* and m_h^* values are the effective masses, μ_{xy} is the reduced x-y plane electron-hole mass and $\rho = \rho_e - \rho_h$ is the relative motion within the quantum well plane. Dismissing the difference in the dielectric constants for well and barrier, the Coulomb potential is

$$V_C(\rho, z_e - z_h) = -\frac{e^2}{\varepsilon\sqrt{\rho^2 + (z_e - z_h)^2}}. \tag{4}$$

We separate the total wave function Φ into the motion along z and the in-plane motion of the exciton $\phi(\rho)$,

$$\Phi = \Psi(z_e, z_h)\phi(\rho) \tag{5}$$

while retaining Coulomb effects in the growth direction

$$\left\{\sum_{i=e,h}\left[-\frac{\hbar^2}{2m_i^*}\frac{\partial^2}{\partial z_i^2} + V_i(z_i)\right] + W(z_e - z_h)\right\}\Psi(z_e, z_h) = i\hbar\frac{\partial}{\partial t}\Psi(z_e, z_h) \tag{6}$$

The potential

$$W(z)=\int_0^\infty d\rho\rho\left[\frac{\hbar}{2\mu_{xy}}\left[\partial_\rho\phi(\rho)\right]^2-\frac{e^2}{\varepsilon\sqrt{\rho^2+z^2}}\phi^2(\rho)\right] \tag{7}$$

will be added to the heterostructure potentials [7]. This two-variable Schrödinger equation can be simplified introducing the factorization $\Psi(z_e,z_h)=\psi(z_e)\psi(z_h)$ and thus, obtaining the equations,

$$\left[-\frac{\hbar^2}{2m_e^*}\frac{\partial}{\partial z_e^2}+V_e(z_e)+W_h(z_e)-eFz_e\right]\psi_e(z_e)=i\hbar\frac{\partial}{\partial t}\psi_e(z_e) \tag{8}$$

$$\left[-\frac{\hbar^2}{2m_h^*}\frac{\partial}{\partial z_h^2}+V_h(z_h)+W_e(z_h)-eFz_h\right]\psi_h(z_h)=i\hbar\frac{\partial}{\partial t}\psi_h(z_h) \tag{9}$$

that have to be solved together since the term

$$W_i(z)=\int dz'\,\psi_i^2(z')W(z-z') \tag{10}$$

couples ψ_e and ψ_h where $i=e,h$. To simplify this calculation we have used the ansatz [8] $\phi(\rho)=(2/a)\,e^{-\rho/a}$ for the in-plane motion of the exciton, where a corresponds to the Bohr radius in the two dimensional case.

The numerical integration in time allows us to obtain the average electron and hole positions, $\langle z\rangle_{ab}^{e,h}$, and the carrier charge density, $Q_{ab}^{e,h}$, in a defined semiconductor region [a,b] at any time t,

$$\langle z\rangle_{ab}^{e,h}(t)=\int_a^b dz_{e,h}\left|\psi^{e,h}(z_{e,h},t)\right|^2 z_{e,h} \tag{11}$$

$$Q_{ab}^{e,h}=\int_a^b dz_{e,h}\left|\psi^{e,h}(z_{e,h},t)\right|^2 \tag{12}$$

Since $z^{e,h}$ depend on t, the Coulomb interaction, which mostly determines the exciton binding energy together with the in-plane kinetic term, will depend on t too. To calculate the binding energy $E_b(t)$ we proceed as follows: at each t and $\langle z\rangle_{ab}^{e,h}(t)$ values $V_C(\rho, z_e\text{-}z_h,t)$ and $W_h(z_e,t)$ are assessed. In this way, the exciton binding energy is given by [9]

$$E_b(t)=\frac{\hbar^2}{2\mu_{xy}a^2}-\frac{4e}{a^2}\int_{z_e}dz_e\psi_e^2(z_e,t)\int_{z_h}dz_h\psi_h^2(z_h,t)\int_0^\infty\rho d\rho V_C(\rho,z_e,z_h t)e^{-2\rho/a}= \tag{13}$$
$$=\int_{z_h}dz_h\psi_h^2(z_h,t)W_e(z_h,t)$$

Two differences exist between the motion of the two kinds of electrons because of the Coulomb interaction. First, the electron-in-exciton oscillations have a more remarkable asymmetry than the free electron oscillations. Second, the period of the former electron is about a 10% greater than that of the latter (29 fs and 26 fs, respectively) in agreement with the calculations of Mohaidat et al. [10]. The electron is accelerated when moving toward the hole and attracted when moving away from the hole. The transition from spatially indirect to spatially direct exciton varies the Coulomb interaction and the in-plane kinetic energy. The exciton binding energy grows abruptly, from 5.1 meV to 11.2 meV, when the spatially indirect exiton changes to the direct one as shown in Fig. 2. This feature is also perceptible in the electron charge density oscillations $Q_{ab}^{e}(t)$ represented in Fig. 3. Thus, we have an oscillating electron-hole distance, whose amplitude is also oscillating in time in a different way from that of the resonant free electron or the electron trapped only by the Coulomb interaction.

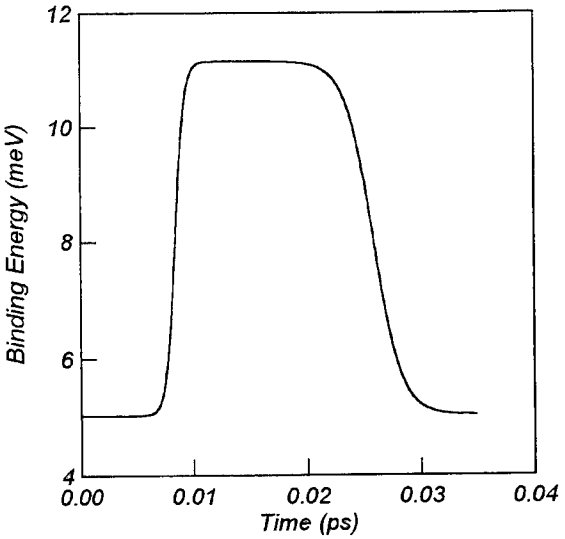

Figure 2. Exciton binding energy versus time during a period. The initial state corresponds to the spatially indirect exciton in the left well.

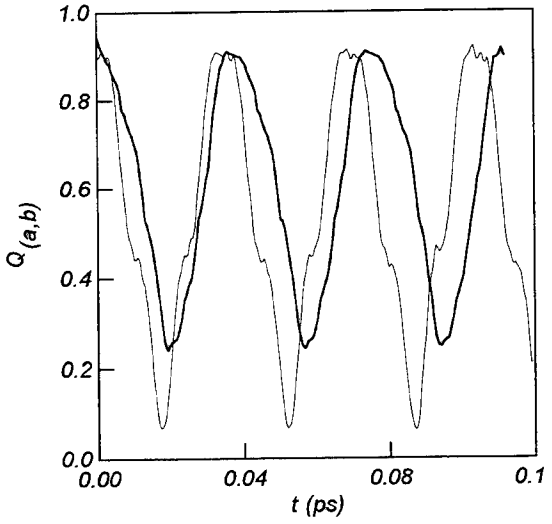

Figure 3. Free electron charge density oscillations (thin line) compared with electron-in-exciton charge density oscillations (thick line) in the left well.

In summary, we have studied the dynamics of a directly created electron-hole pair in an asymmetric double quantum well system. This exciton is generated through hole-assisted electron resonant tunneling, being a two-particle process. The excitonic dynamics is basically determined by the two different natures of the exciton (spatially indirect and spatially direct exciton) . The electron-in-exciton asymmetic charge oscillations, together with the confined hole, lead to a new type of coherent radiation emerging from the semiconductor ACQW, after electrical pumping. Taking into account that the mean life for an electron-hole pair in $In_{0.53}Ga_{0.47}As$ is about 300ps, an experimental observation of such a process is possible in principle.

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Future Direction: Advanced Concepts

SCHOTTKY BARRIER MOSFETS FOR SILICON NANOELECTRONICS

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Metal silicide source/drain MOSFETs may provide a simple route to terabit integrated circuits with ~25nm gate length and ~100nm overall device size. Potential advantages of this approach are outlined here along with recent progress.

All commercial silicon transistors today employ p-n junctions to confine carriers and control the flow of current. At nanometer dimensions, however, depletion widths are much too large to be accommodated at any channel doping light enough to prevent tunneling, so that future device structures will need to be radically altered as minimum feature sizes are reduced below 0.1μm. Thus far there is no consensus on how this will be accomplished.

Silicon-on-insulator (SOI) provides an opportunity for improved scaling and reduced junction capacitance, but ultra-thin SOI having the required uniformity may prove difficult and costly to produce. Bulk n-channel MOSFETs have recently been demonstrated to gate lengths of ~40nm by employing exotic methods to fabricate ~10nm-deep source and drain extensions.[1] Integrating these structures into practical high-density ICs, however, poses many process difficulties and one fundamental problem. At gate lengths of ~50nm or less, random locations of dopants within a conventional MOSFET channel cause significant variations in threshold voltage and output characteristics for device widths comparable to the gate length. This difficulty has led to recent proposals which eliminate dopants from the channel through use of a bottom gate in addition to the top gate, in order to control the channel potential over ~30nm dimensions.[2,3] This poses another set of difficult processing problems, however, by requiring lateral phase epitaxy to grow crystalline silicon channels over the bottom-gate oxide.

Aside from technical difficulties, each of these approaches retains heavily-doped source and drain regions within an all-silicon homojunction device. This, in itself, poses a problem for scaling to nanometer dimensions. Metal contacts form Schottky barriers to source/drain regions with depletion widths of ~30Å at typical doping densities of $\sim 10^{20}cm^{-3}$. The associated tunneling resistance increases as the inverse square of the scaling parameter, while effective channel conductance remains nearly constant (for approximately constant electric fields). The total area of homojunction FETs can therefore not be scaled to nanometer dimensions unless active doping densities of $\sim 10^{21}cm^{-3}$ can be used to make Schottky barrier contacts semi-transparent.

Overall size for future nanoscale transistors is crucial to their circuit performance. Smaller total area increases integration levels, reduces parasitics, and provides shorter local interconnects. Shorter gate length alone is not enough, since most of the area on today's chips is taken up with contacts and isolation. Simplicity of fabrication is also crucial. Process complexity for advanced CMOS is increasing at a rate which could threaten the economics of downsizing well before technical limitations are reached. Innovations which reduce transistor area and simultaneously simplify processing are thus potentially very valuable.

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A simple approach to meet these challenges is the substitution of metal silicides for heavily-doped silicon within the source/drain regions of otherwise conventional MOSFETs. Metal silicides form natural Schottky barriers to silicon substrates which act to confine the carriers, reducing or eliminating the need for dopant impurities in the channel to prevent current flow in the "off" condition. Sub-surface isolation can also be eliminated because latch-up is impossible. Schottky barrier (SB) MOSFETs are turned "on" by large gate-induced electric fields at the top of the source electrode which induce internal field emission (Fowler-Nordheim tunneling) through the Schottky barrier and into the silicon channel, similar to the reverse tunneling currents observed in heavily-doped Schottky diodes. The original idea for metal silicide source/drain goes back to a 1968 paper by Lepselter and Sze.[4] Gate-induced tunneling could not be realized in their device, however, due to a large lateral gap between gate and source electrodes, and field emission was observed only at low temperatures by application of large drain voltages to enhance the source electric field. There was further experimental interest in the early days of CMOS due to latch-up immunity, but drain currents in these devices resulted from thermionic emission *over* the Schottky barrier rather than gate-induced tunneling *through* the barrier and were insufficient for circuit applications.

During the past four years, the idea of gate-induced tunneling has been advocated independently by several groups as a means to improve scaling.[5,6,7] Heterojunction source barriers inhibit punch-through and drain-induced barrier lowering, permitting much shorter gate lengths in bulk devices. In 1994, my group proposed the undoped PtSi SB-MOSFET structure[8] illustrated in Fig. 1. Unknown to us, the same device was already in fabrication at Stanford/ HP Palo Alto by Snyder, Helms, and Nishi.[9] Measured results on their L≈1μm gate length devices confirmed all aspects of the expected behavior in semi-quantitative agreement with our simulations.

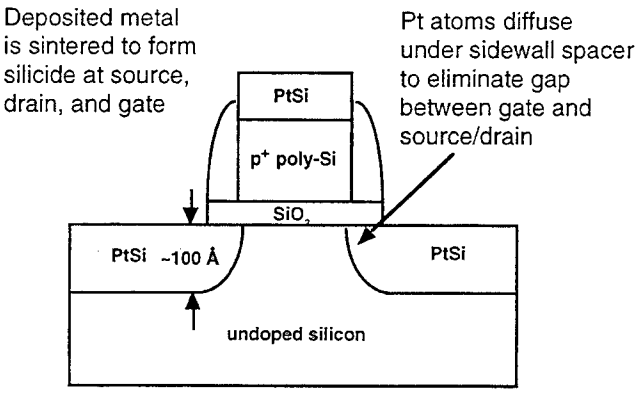

Fig. 1 Schematic illustration of undoped p-type PtSi Schottky barrier MOSFET.[8]

Preliminary simulations for undoped PtSi SB-MOSFETs with L=50nm and 3.5nm gate oxide are shown in Fig. 2. This p-channel device utilizes the low p-barrier, $\Phi_B^p \approx 0.25$eV, for PtSi. A complementary device employing the low n-barrier for $ErSi_2$, $\Phi_B^n \approx 0.28$eV, yields similar results with larger drain currents due to the lighter electron mass. Gate voltages are relative to flat-band in these simulations. With dual p^+- and n^+-polysilicon gates, applied gate voltages are reduced by the height of the Schottky barrier to yield well-matched thresholds $V_T \approx \pm 0.35$V and a supply voltage of ~1.5V. SB-MOSFETs are turned "on" by electric fields which render the source barrier semi-transparent, so drain currents in Fig. 2 are similar to experimental 0.1μm CMOS with 3.5nm oxides. Actually, we expect substantially larger drain currents than shown here due to ballistic

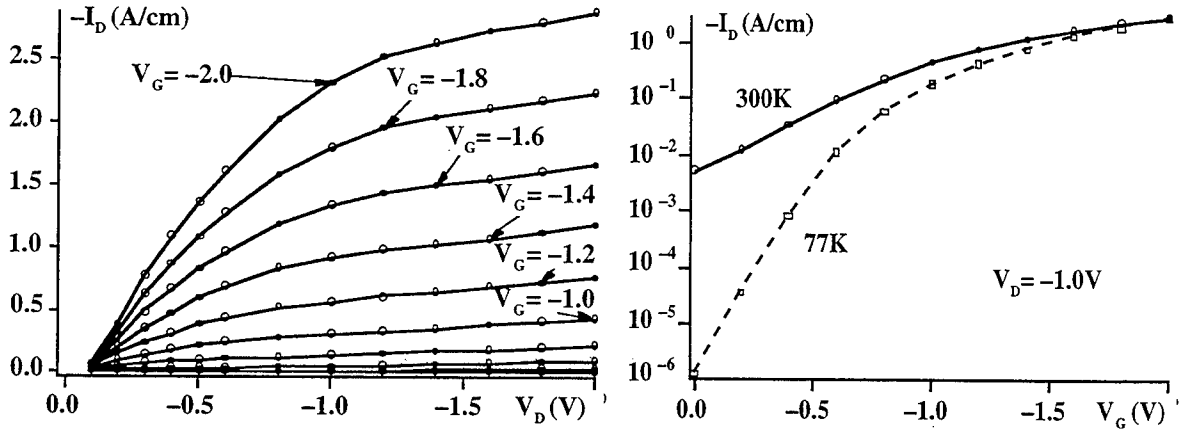

Fig. 2 Preliminary simulations of drain characteristics for an undoped PtSi SB-MOSFET with gate length L=50nm and oxide thickness t_{ox}=3.5nm. Gate voltage is relative to flat-band.

effects in such short channels, and more accurate Monte Carlo simulations are now in progress. Subthreshold characteristics in Fig. 2 show a turn-off ratio of ~10^6 at 77K, but only ~200 at room temperature. Thermal emission can be greatly suppressed, however, by employing metal gates of different work function in combination with relatively light substrate doping. This approach has been demonstrated recently at IBM in a novel T-gate SB n-MOSFET by Rishton, Ismail, Chu, and Chan[10] showing good room temperature performance with >10^8 turn-off ratio in a 0.25μm device.

Gate length and supply voltage for SB-MOSFETs can be further reduced by using thinner oxides (~2nm), higher dielectric constant insulators (e.g. Si_3N_4), or lower barrier silicides (e.g. IrSi). In the example of Fig. 2, devices with 2.0nm equivalent oxide thickness would yield similar characteristics at 28.5nm gate length and 0.85V supply voltage. Commercial ICs with 2nm oxides and ~1.0V supply are expected in the next few years, so that bulk SB-MOS should scale easily into the ~25nm regime with advances in lithography and processing.

Figure 3 sketches a future ~25nm gate-length CMOS employing metal gates of optimized work function in combination with buried, epitaxial, and self-planarized $CoSi_2$ local interconnects[11] put down by selective metal deposition and annealing prior to device fabrication. Lines beneath each device indicate optional regions of moderate doping (fully depleted) which can be added to suppress thermal emission for room temperature operation. In the end, the successful approach to nanometer device scaling is likely to be the one most easily fabricated. The striking simplicity of SB-MOS can be inferred from the sketch of Fig. 3 and the following list of potential advantages.

(1) Fabrication is greatly simplified:
- all or most impurity doping is eliminated.
- sub-surface isolation is not required; latch-up is impossible.
- field oxide can be deposited and patterned, eliminating trenches and LOCOS.
- silicide source/drain can be incorporated into local interconnects, reducing contact area.

(2) Short-channel effects are suppressed:
- ultra-shallow silicide source/drain is easily achieved.

field emission confines tunneling to top ~2nm of the source electrode.
Schottky barriers prevent punch-through and drain-induced barrier lowering.
short-channel effects occur by drain-enhanced tunneling only at L<30nm for t_{ox}=2nm.

(3) Device density is greatly increased:
elimination of (most) doping, wells, sub-surface isolation, body contacts, and merging of source/drain regions and common CMOS nodes with local interconnects yields much higher density at any minimum feature size.
reduced short-channel effects permit scaling far beyond limits of conventional bulk devices.

(4) Circuit speed is also increased:
source/drain junction capacitance and sheet resistance are effectively eliminated.
zero doping eliminates interconnect capacitance to substrate.
higher packing density yields shorter local interconnects.
body effect is eliminated, improving speed in low-voltage circuits with pass transistors and stacked gates.

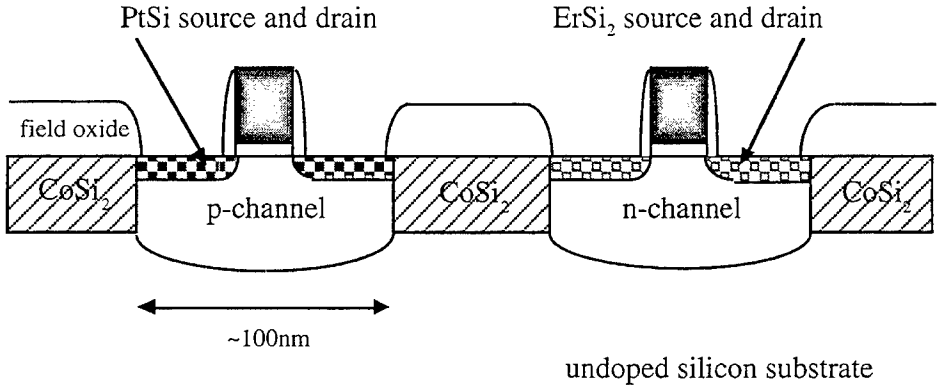

Fig. 3 Sketch of future ~25nm gate-length Schottky barrier CMOS inverter with buried, epitaxial, and self-planarized $CoSi_2$ local interconnects.

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TOWARD ROOM TEMPERATURE OPERATION AND HIGH DENSITY INTEGRATION OF SINGLE ELECTRON DEVICES

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Main features and limitations of present LSIs and emerging quantum LSIs are briefly discussed. As the next-generation electronics, quantum LSIs based on single electron devices on quantum dot arrays are most promising. Key issues for success of their room temperature operation and high density integration are discussed.

1. Limitations of Present-Day LSI Architecture

The system architecture of present LSI is predominantly based on the Boolean logic. The device architecture to implement such a system architecture consists of an array of transistor switches. Transistors in digital circuits predominantly operate only as simple, small and robust switches of lumped nature in spite of their sophisticated distributed structures. It is well known that the operation principle of such transistors is based on "classical particle" picture of electrons and holes. LSI technology has made a tremendous progress in the latter half of this century, particularly in terms of the integration level. This progress has been brought about predominantly by miniaturization or scale-down of device feature size. The technological trend extrapolates itself to production-level realization of structures with the feature size of about 100 nanometer or below around the end of this century, approaching de Broglie wavelength of the electrons in solids.

However, it is now anticipated that this simple and powerful architecture will, upon further miniaturization, encounter serious difficulties and leads to saturation in integration level. The major limiting factors include; (1) material and processing related limitation(doping fluctuation, avalanche, MOS interface instability, electromigration, stress-migration, interface reaction etc.), (2) power limitation, (3)wiring limitation, (4) quantum mechanical limitation (quantum fluctuation, failure of device and device isolation due to tunneling), and (5) system architecture limitation. It should be noted that most of these factors are more or less direct consequences of the switch- array device architecture where all the individual switches should be interconnected, and each switch, however small it is, should possess a sufficient current-drive capability to charge not only the input capacitances of the next switches but also the interconnect capacitances. The limited system-architecture capability of the present switch-array device architecture is also becoming an issue. It has been found that the present device architecture, which has been so successful with von-Neumann architecture with Boolean logic, is not suitable or extremely inefficient for implementing system applications such as neural networks, artificial intelligence, knowledge machines and video image processing where non-von-Neumann types of system architectures with massively parallel processing are involved.

2. Quantum Devices Utilizing Quantum Nanostructures

On the other hand, such a miniaturization capability in turn allows one to control quantum mechanical wave-particle duality of each electron by utilizing artificial nanostructures, and opens up a possibility of constructing a "quantum LSIs" based on quantum devices.In the quantum nanostructures such as quantum wells, wires and dots, new physical phenomena resulting from the wave-particle nature of electrons appear. The main effects which are interesting from the view-point of device applications include; (1)formation of new confined quantum states with new energy level spectra, (2)formation of new coupled quantum systems, (3)single- and multi- mode transport of electron waves, (4)field control of wavelength and phase of electron waves, (5)diffraction and

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Bragg reflection, (6)tunneling and resonant tunneling and (7)Coulomb blockade.

Utilizing these effects, many kinds of devices with new functions have been proposed[1]. Since each electron manifests either wave-nature or particle-nature predominantly depending on its environment, one can envisage two kinds of devices in the quantum regime, i.e., "quantum wave devices" and "single electron devices". In the former, electrons are put into some kinds of phase-coherent structures and their wave properties are utilized. Examples include; (1)quantum wire transistors, (2)electron lenses, reflectors and deflectors, (3)quantum interference devices using waveguide structures, (4)electron Bragg reflectors and superlattice devices, (5)resonant tunneling devices. These devices posses analogy to various devices in optics and microwave electronics such as Fabry-Perot resonators, Mach-Zehndar and Michelson interferometers, thin-film multi layer filters, microwave couplers and filters, etc. On the other hand, in the single electron devices (SEDs), electrons are put into dot structures and their particle-nature is emphasized where discrete nature of electron charge plays an important role. For example, an extremely small electrostatic energy change caused by transfer of a single electron can block the tunneling process itself (Coulomb blockade) in ultra-small tunneling junctions. Thus, by having two ultra-small junctions attached to a quantum dot together with an external control gate to cause or remove Coulomb blockade, one can construct a single electron transistor (SET)[2,3].

Thus, there are many kinds of quantum devices and it is difficult at present to comment decisively which device is viable for future quantum LSIs. Traditional criteria for switching devices include operation temperature, three terminal nature, signal amplifying capability, output drive capability, impedance matching to wiring, noise immunity, device uniformity, device size, structural simplicity, operation stability etc. However, these criteria are very much dependent on the device/system architecture. The weakest point of the quantum devices at present is the operation temperature. At present, only resonant tunneling devices work at room temperature and single electron devices have good prospect of working at or close to room temperature. Except this, all other devices mentioned above operate at a low temperature range from several hundred mK to 10K because of short phase coherent length and/or small separation of energy levels of confined quantum states.

3. Key Issues and Efforts for Room Temperature Operation and High Density Integration of Single Electron Devices

The single electron device can be regarded as an ultimate form of the electronic device. Their potential integration level is extremely high due to its small size and its expected low speed power product close to the quantum limit set by the Heisnberg's uncertainty principle[4]. Recently, prospect of room temperature operation has been demonstrated in ultra-narrow Si wire based SETs[5] and metal-based SETs[6]. Room-temperature single electron memory using a ploy-Si granular structure is also being developed[7]. Due to these, intensive attentions are currently being paid to single electron devices, and systematic research efforts are being made to investigate the feasibility of these devices as a serious candidate for the next-generation electronics.

Among them is the Scientific Research Project on Priority Area of "Single ELectron Devices and Their High Density Integration" started in Japan from April 1996 for a period of 4 years. In this Project, about 50 professors in Japanese Universities will collaborate over the research topics of(1) fundamental physics of quantum dots and their formation, (2)surface and interface control of quantum dots for optimal single electron transport,(3)single electron deices, circuits and architectures,and(4)high density integration of quantum dots and single electron devices. Roughly speaking, key issues related to nanofabrication and to device/circuits/system architecture are addressed in this project. Present status of these issues is briefly reviewed below:

3.1 Nanofabrication Issues

(a)fabrication methods: For quantum LSIs working at room temperature, high density arrays of dots with sizes small enough (below 10 nm) are required. Current formation approaches include; (1) direct fabrication of electron confinement region by application of standard Si ULSI processing technologies, such as EB lithography and dry etching to silicon wafers, (2) direct application of standard Si ULSI processing technologies such as above to epitaxialy-grown quantum well wafers of compound semiconductors, (3) selective depletion of two-dimensional electron gas (2DEG) in compound semiconductor by surface potential modulation of semiconductor using Schottky gate, MIS gate, etc, (4) direct fabrication of nanostructures by scanned probe-induced atom-manipulation and surface reaction, (5) realization of wire or dot structures based on the self-organizing growth mechanism in MBE or MOVPE growth of compound semiconductors, and (6) formation of ultra-fine particles by CVD process and various molecular reactions.

Among them, the first and second approaches are most practical if they work sufficiently well. However, process- induced damages are serious as well as achievable feature size are not quite small enough with rugged interfaces. The third approach largely solves these problems while maintaining the advantages of the second approach. Confined regions can be formed far from the surface and deep in the high quality crystal in a gate controlled fashion, and the isotropic feature of Coulomb force quickly smears the ruggedness of the surface. However, with standard split gate geometry, achievable confinement potential is usually too weak for room temperature operation of devices. In-plane-gate and wrap gate geometries recently proposed by the author's group[8] improve the situation. The forth approach is very good for research on discrete level devices, but utterly impractical at present for high density integration of many devices. Thus, the fifth and sixth approaches are being intensively studied all over the world. Examples of the fifth approach include selective growth on mesa-patterned substrates, area-selective growth using patterned insulator windows, self-organized growth utilizing step bunching on vicinal substrates, Stranski-Krastanow (SK) mode driven self-assembly of dots, strain-driven self- organized disk formation on high-index substrates, etc. As an example, the fifth approach has led to successful realization of quantum dot-wire networks by selective MOVPE growth[9]. Using the sixth approach, small and uniform silicon nanoparticles have been realized with observation of Coulomb staircases at room temperature[10].

(b)surface/interface control: One major nanofabrication issue lies in the control of surfaces and interfaces of quantum structures. Homo-, hetero-, MOS and Schottky interfaces, which are essential constituent elements in the present-day devices and control classical motions of carriers, should now control the wave-particle properties of each electron in the single electron devices. Due to reduced dimensions and different roles of the interfaces, interfaces play far more important roles in SEDs. Thus, the interfaces of quantum structures should be perfect in the interface atom arrangements and be capable of producing desired potential profiles required for SED operation. Additionally, the interface region should be free of ionized impurities and trapping defects such as surface states, interface states and discrete deep levels. In this connection, the author's group has recently succeeded in removing Fermi level pinning and surface state effects from AlGaAs/GaAs near surface quantum wells and InAlAs/InGaAs wires[11], using a silicon interlayer based surface passivation technique.

3.2 Device/Circuit/System Architecture Issues

As for the device/system architecture of SED LSIs, nothing has so far been established, and various possibilities are presently being explored. Obviously, one can think of the following three alternatives for possible architectures; (1) conventional Boolean logic based von Neumann type

architecture implemented with conventional SET switch-array device architecture with improved integration level and speed-power performance, (2) conventional Boolean logic system architecture with a new device architecture utilizing SEDs with increased functionality than switches, and (3) non-Von Neumann architecture with new device architecture utilizing SEDs with increased functionality. Although the first approach is currently investigated most intensively, second and third alternatives seem to offer more improvements over the first.

In nm-scale quantum dot structures, the classical charging effect, quantum confinement effect, electron-electron interaction, tunneling effects etc. exhibit interesting interplay, and they provide unexplored new possibilities for new functional devices and new architecture LSIs. As an example, in an one-dimensional and two-dimensional arrays of dots with tunneling junctions, electrons propagate like solitons, and this may be used as wiring or to implement certain type of special information processing. It has been shown theoretically that cellular automata can be constructed by chain of sets of five single electron dots[12]. Recently, binary decision device arrays[13] and cellular automata based on more conventional tunnel junctions[14] have been proposed. For the successful development of "Single Electronics", intensive collaboration efforts between researchers in the material and device related fields such as basic physics, electron device physics, material science, processing engineering, etc, and those in the system related fields such as circuit and system engineering, computer science, neural networks, etc, seem to be vitally important.

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Plasma Wave Electronics: Terahertz Detectors and Sources Using Two Dimensional Electronic Fluid in High Electron Mobility Transistors.

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Abstract.

We discuss applications of plasma waves in High Electron Mobility Transistors for detectors and sources operating in millimeter and submillimeter range. A short channel High Electron Mobility Transistor (HEMT) has a resonance response to electromagnetic radiation at the plasma oscillation frequencies of the two dimensional electrons in the device. The devices, which use this resonance response should operate at much higher frequencies than conventional, transit-time limited devices, since the plasma waves propagate much faster than electrons. The responsivities of such devices may greatly exceed the responsivities of Schottky diodes currently used as detectors and mixers in the terahertz range. A long channel HEMT has a nonresonant response to electromagnetic radiation and can be used as a broad band detector for frequencies up to several tens of terahertz. Recently, a prototype non-resonant detector (operating in the microwave range) was fabricated using an AlGaAs/GaAs 0.15 micron gate HEMT. The measured dependencies of the detector responsivity on the gate bias and frequency are in good agreement with our theory.

Introduction.

In this paper, we review our recent work [1-6] on the applications of plasma waves in High Electron Mobility Transistors for detectors and sources operating in microwave, millimeter and submillimeter range. Plasma waves in a FET have a linear dispersion law, just like sound waves. The plasma wave velocity in a FET can easily exceed 10^8 cm/s (about an order of magnitude higher than the electron saturation velocity in GaAs or Si). That is why plasma wave electronics will operate at much higher frequencies than conventional electronics (for a 0.1 micron FET the operating frequency will be in a terahertz range). A field effect transistor channel acts as a resonance cavity for plasma waves. The quality factor of such a cavity is on the order of $Q = sL/\tau$ where L is the channel length, and t is the momentum relaxation time. In a high mobility, short channel FET, this quality factor can easily exceed 10. In a FET with a small DC current, plasma waves may grow and this leads to the emission of far infra-red radiation. A plasma wave instability may occur due to the boundary conditions typical for a FET, which lead to plasma wave amplification due to reflections from the drain

The nonlinear hydrodynamic properties of the electron fluid may be used for new types of detectors, mixers, and amplifiers. A short channel High Electron Mobility Transistor (HEMT) has a resonance response to electromagnetic radiation at the plasma oscillation frequencies of the two dimensional electrons in the device. A long channel HEMT has a nonresonant response to electromagnetic radiation and can be used as a broad band detector for frequencies up to several tens of terahertz. Our estimates show that the sensitivity of the resonant HEMT detector should exceed the sensitivity of conventional Schottky diode detectors by a factor of Q^2, that is by several orders of magnitude. The sensitivity of the non-resonant, broad band HEMT detector is comparable to the sensitivity of conventional Schottky diode detectors (approximately 600 V/W).

Basic equations

As was discussed in [4], for a highly non-ideal electron gas in an AlGaAs/GaAs heterostructures with the electron surface concentration, n_s, on the order of 10^{12} cm^{-2} at 77 K, the thermal energy, the Fermi energy, and the Bohr energy are of the same order. Under such conditions, the mean free path for electron-electron collisions ($\approx$ 100 Å) is much smaller than both the mean free path and a typical gate length, and the hydrodynamic approach should be adopted.

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The basic equations describing the two dimensional electronic fluid are the relationship between the surface carrier concentration and gate voltage swing, the hydrodynamic equation of motion, and the continuity equation. The surface concentration, n_S, in the FET channel is related to the local gate-to-channel voltage swing, $U = U_{gc}(x) - U_T$, by

$$n_S = CU / e \tag{1}$$

where C is the gate capacitance per unit area and $U_{gc}(x)$ is the local gate-to-channel voltage. Eq. (1) represents the usual gradual channel approximation [7] which is valid when the characteristic scale of the potential variation in the channel is much greater than the gate-to-channel separation.

The equation of motion (the Euler equation) is

$$\frac{\partial \mathrm{v}}{\partial t} + \mathrm{v}\frac{\partial \mathrm{v}}{\partial x} + \frac{e}{m}\frac{\partial U}{\partial x} + \frac{\mathrm{v}}{\tau} = 0 \tag{2}$$

where $\partial U/\partial x$ is the longitudinal electric field in the channel, $\mathrm{v}(x,t)$ is the local electron velocity, and m is the electron effective mass. The last term accounts for electronic collisions with phonons and/or impurities. (Here we neglect the viscosity of the electronic fluid.) Eq. (2) has to be solved together with the usual continuity equation which (taking Eq. (1) into account) can be written as :

$$\frac{\partial U}{\partial t} + \frac{\partial (U\mathrm{v})}{\partial x} = 0 \tag{3}$$

Equations (2) and (3) coincide with the equations describing the shallow water in conventional hydrodynamics if U is replaced by the water level and e/m is replaced by the free fall acceleration.

Another important parameter is viscosity. The viscosity of the 2D electronic fluid is of the order of $\mathrm{v}_F\lambda_{ee}$ where v_F is the Fermi velocity and λ_{ee} is the mean free path for the electron-electron collisions, which is on the order of the inter-electronic distance, $n_S^{-1/2}$. Then we obtain the following estimate for the viscosity of the electron fluid: $\nu = \hbar / m \approx 15$ cm^2/s for GaAs. For comparison, the viscosity of air is about 0.15 cm^2/s.

Electronic Flute and Terahertz Sources.

It is well known that plasma waves with a linear dispersion law, $\omega = sk$, may propagate in a Field Effect Transistor channel. [8-10] Here ω is frequency, $s = (eU/m)^{1/2}$ is the wave velocity, e is the electronic charge, m is the electron effective mass, U is the gate-to channel voltage swing, and k is the wave vector. Allen et al. observed infrared absorption [11] and Tsui et al. observed weak infrared emission [12] related to such waves in silicon inversion layers.

As discussed in [13], plasma waves are similar not only to shallow water waves but also to sound waves since they have a linear dispersion law. In turn, shallow water behavior is similar to the dynamics of a gas with pressure proportional to the square of the density, (see, for example, [14]). Thus, the nonlinear hydrodynamic equations for the 2D electron fluid are similar to (but not identical with) the equations for a real gas, such as air. However, the linearized equations describing small-amplitude plasma waves in a FET and sound waves in a gas are identical. Since the linearized equations determine the instability threshold for a steady flow (i. e. the wave generation threshold), the instability conditions for a real gas and for a 2D electron fluid should be similar provided that the Reynolds numbers and quality factors of resonance cavities are the same. Hence, one can design a device, which we called an "electronic flute" [3]. In [3], we showed that these dimensionless parameters for our "electronic flute" should be of the same order of magnitude as for a conventional flute.

In a short field effect transistor where electrons experience practically no collisions with

phonons and/or impurities during the transit time (we call such a device a Ballistic FET). However, the high electron concentration results in many electron-electron collisions. In this case, individual electrons cannot be considered as ballistic particles but the two dimensional (2D) electron gas as a whole will exhibit interesting hydrodynamic behavior. As we showed in [4], the steady state of a current-carrying Ballistic FET is unstable for appropriate boundary conditions.

As a consequence of the instability, the amplitude plasma oscillations grows in time, reaching a steady-state amplitude determined by sheet carrier concentration in the channel, momentum relaxation time, and device length. [15] This results in a periodic variation of the channel charge and the mirror image charge in the gate contact, i. e. to the periodic variation of the dipole moment. This variation should lead to electromagnetic radiation. The device length is much smaller than the wavelength of the electromagnetic radiation, λ_R at the plasma wave frequency. (The transverse dimension, W, may be made comparable to λ_R.). Hence, the Ballistic FET operates as a point or linear source of electromagnetic radiation. Many such devices can be placed into a quasi-optical array for power combining. The maximum modulation frequency is still limited by the transit time ($\approx$ 2 ps in our example).

Detection and Mixing of Terahertz Radiation by Two Dimensional Electronic Fluid

As we discussed above, plasma waves may be coupled to electromagnetic radiation. Conversely, electromagnetic radiation can excite plasma waves, and, therefore, a FET has a resonance response at the plasma wave frequency. The half width of the resonance curve is determined by the inverse momentum relaxation time. As we discussed in [1, 2], this effect can be used for the resonance detection and mixing of electromagnetic radiation at terahertz frequencies.

We also showed that at low frequencies, ω, such that $\omega\tau << 1$, where τ is the momentum relaxation time, the HEMT works as the detector of electromagnetic radiation with the responsivities, which are comparable to those of Schottky diode detectors. In the low frequency limit, our theory predicts that the responsivity, R, of such a HEMT detector is given by

$$R = \alpha L^4\omega^2/(6s^4\tau^2)$$

The pre-factor α depends on the boundary conditions.

Recently, we fabricated a prototype non-resonant detector (operating in the microwave range) using a AlGaAs/GaAs 0.15 micron gate HEMT. [6] The measured dependencies of the detector responsivity on the gate bias and frequency were in good agreement with our theory (see Fig. 1).

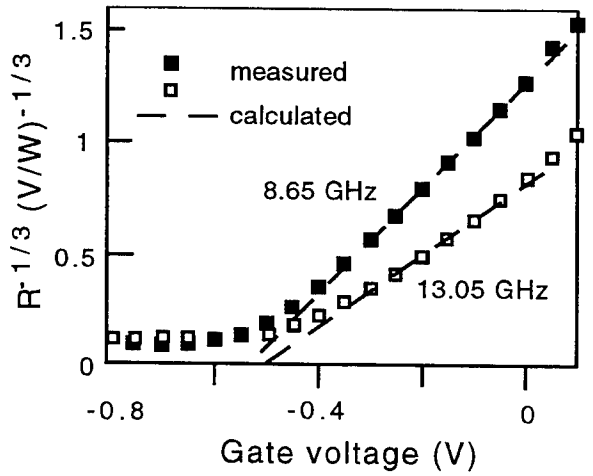

Fig. 1. Comparison of measured and predicted responsivities for an AlGaAs/GaAs HEMT. [6]

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High Temperature Operation of Narrow Channel AlInAs/InGaAs/AlInAs 3D-SMODFETs for Power Amplifiers

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Abstract

Using a modulation doped field effect transistor (MODFET) with a pseudomorphic parabolically graded channel and atomic planar doped pseudomorphic barriers on both sides of the channel, it is possible to achieve record-breaking electron sheet densities in the channel without having carriers in the barrier (Double-Doped Double-Strained MODFET, 3D-SMODFET). Designing double-doped MODFETs with stress compensation allows the total thickness of all the pseudomorphic layers to be extended beyond any one critical layer thickness value. Using a simple analytical method, an optimum material structure for AlInAs/InGaAs/AlInAs 3D-SMODFETs with narrow full channels will be shown. These narrow channel 3D-SMODFETs on InP show minimal short channel effects (output conductance < 15 mS/mm) at elevated temperatures with good pinch-off characteristics and RF performance (f_{MAX} to f_T ratio of 3).

Introduction

AlInAs/InGaAs MODFETs on InP have demonstrated their potential for high frequency performance [1], but generally have been limited to small signal applications. They have historically been troubled with high output conductance (kink effect), gate leakage and low breakdown voltages. These problems can mostly be related to the non-random alloy clustering of the AlInAs barriers and the impact ionization within the InGaAs channel [2-4]. Various solutions have been applied to the above problems such as the insertion of acceptor doped layers (to increase the vertical fields), AlAs/InAs superlattices (to minimize the non-random alloy clustering) and InP layers (to enhance the barrier to hole current).

By surrounding a narrow compressively strained channel ($In_{.53+x}Ga_{.47-x}As$, $x > 0$) with tensilely strained barriers ($In_{.52-x}Al_{.48+x}As$, $x > 0$) and staying within the critical layer thickness, we can increase the conduction band discontinuity (ΔEc) to greater then 7 eV. This high potential value for ΔEc allows a greater freedom in optimizing the thickness of the quantum well and consequently the channel resistance. Engineering the two-dimensional electron gas (2DEG) to only $n = 1$ states leads us to a concept of narrow quantum wells. Implementing the idea of narrow quantum wells with the AlInAs/InGaAs 3D-MODFETs on InP have resulted in record electron sheet densities with minimal short channel effects at elevated temperatures [5].

The electrical performance of lattice-matched AlInAs/InGaAs MODFETs degrades at high temperatures due to the failure of the Schottky barrier on AlInAs [1]. This failure is due to excess gate leakage as the Schottky barrier decreases with an increase in temperature. By increasing the aluminum concentration (48 to 60 %) in the AlInAs barrier leads to higher Schottky barrier heights (> 1 eV) and a reduced probability of any InAs pipettes [3]. These InAs pipettes in the AlInAs barrier ,can short the gate to the channel (2DEG) causing excessive

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gate leakage and consequently catastrophic device breakdown. By reducing the binary clustering of the AlInAs improves the overall performance of the AlInAs/InGaAs MODFET on InP substrates.

3D-SMODFET Design

We have designed, fabricated, and tested narrow channel 3D-SMODFETs on InP with and without parabolically graded channels [6]. The indium percentage, is increased in the channel (biaxial compression) and is decreased in the barriers (biaxial tension) to increase the conduction band discontinuity. By using successive layers of biaxial tension and compression the net overall stress is reduced as seen in Fig. 1. The thickness of the channel (quantum well) and the conduction band offset determine the quantized energy levels in the channel. By decreasing the thickness of the channel we can raise and separate the quantized energy levels in the channel. Using a simple analytical model [6] the optimized channel thickness for single and double-sided doped MODFETs on InP substrates is shown in Fig. 2.

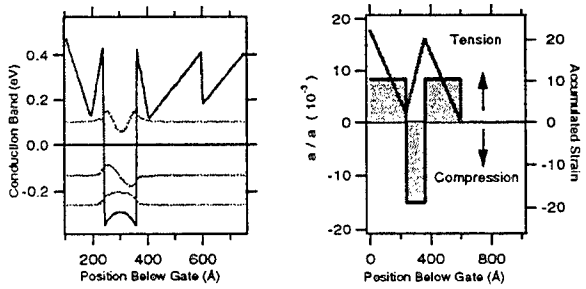

Figure 1 Double modulation doped double-strained MODFET (3D-SMODFET) with stress compensation. The quantum well (120Å) is in compressive strain while the barriers and spacers (240Å) are in tensile strain. The total accumulated stress shows how the compressive strain cancels half of the total tensile strain.

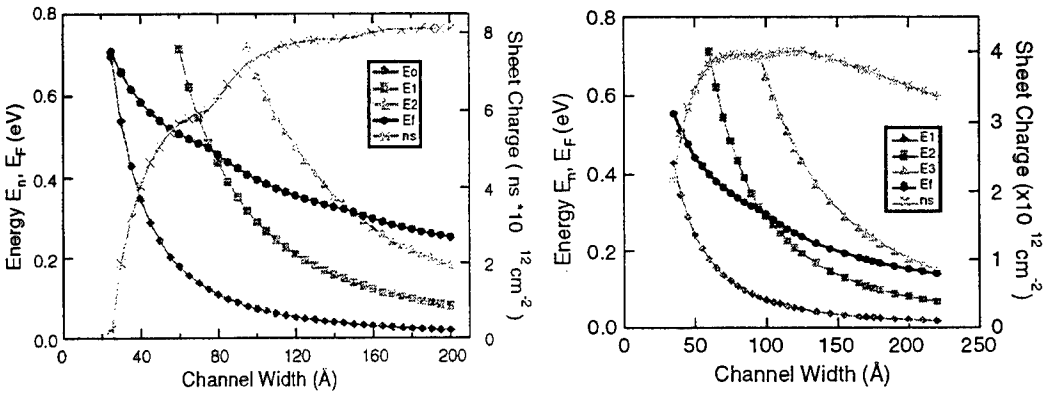

Figure 2 Double and single doped MODFET with Al_6In_4As barriers and $In_xGa_{1-x}As$ channels on InP substrates. The average value of indium in the channel was calculated from the Matthews/Blakslee critical thickness equation. The ground state (diamonds), first excited state (squares), second excited state (triangles), Fermi energy (circles), and the maximum sheet charge (stars) are shown versus channel thickness

Experiment

Using molecular beam epitaxy we grew the 3D-SMODFET structure on Iron doped InP substrates. The devices were grown as follows: 2500 Å of $Al_{0.48}In_{0.52}As$ as a buffer, 200 Å of $Al_{0.6}In_{0.4}As$ as a lower barrier, lower atomic planar doping (APD) of Si, 40 Å of $Al_{0.6}In_{0.4}As$ as a spacer, 200 Å of $In_xGa_{1-x}As$ (x_{av}=.65) for the channel, 40 Å of $Al_{0.6}In_{0.4}As$ as a top spacer, upper APD of Si, 200 Å of $Al_{0.6}In_{0.4}As$ as a Schottky barrier and 100 Å of $In_{0.53}Ga_{0.47}As$ as a cap

doped at 5 x 10^{18} cm^{-3}. Fig. 1 shows the conduction band diagram around the quantum well for a 120 Å channel. The first three wave functions are superimposed at the corresponding quantized energy levels.

The devices were fabricated using a standard mesa isolation, alloyed ohmic contacts and E-beam lithography for the gates. An additional sidewall channel etch was performed to eliminate the gate to InGaAs mesa contact [7]. The ohmic contacts were formed using Ni/AuGe/Ag/Au which was alloyed at 340°C in an RTA for 10 sec producing contact resistances less than 0.1 Ω-mm.

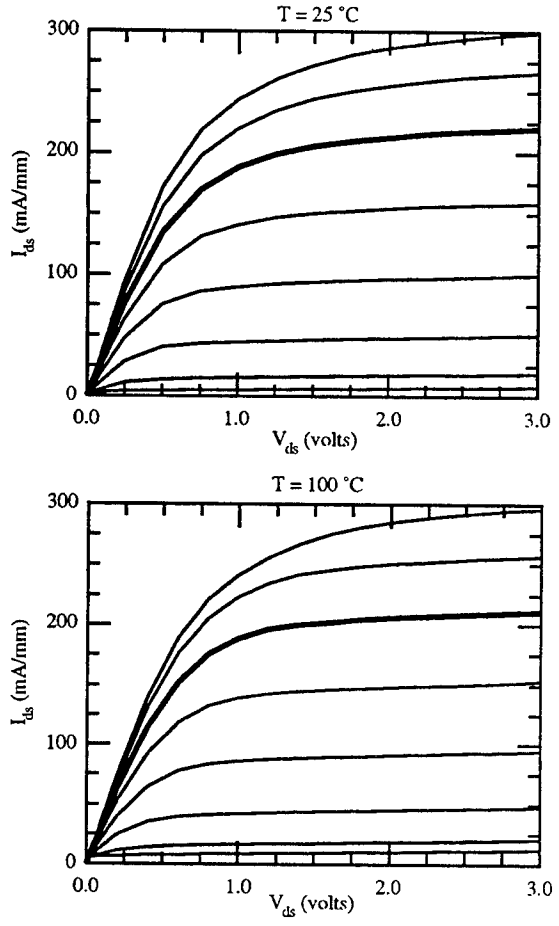

Figure 4 2 µm x 100 µm (L_g x W_g) I_{ds} versus V_{ds} characteristics for a 3D-SMODFET at 25 °C and 100 °C [V_{gs} = +0.5 (top) to -1.25 (bottom) in 0.25 V steps].

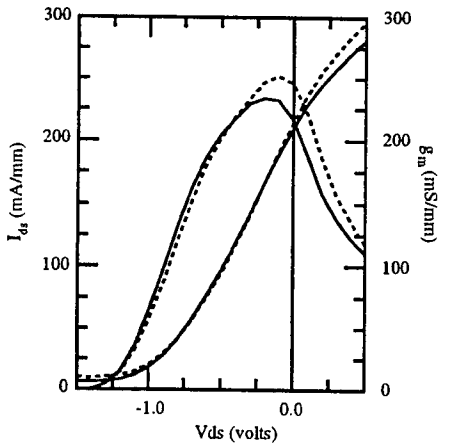

Figure 3 2 µm x 100 µm (L_g x W_g) I_{ds}, g_m versus V_{gs} characteristics for a 3D-SMODFET at 25 °C (solid) and 100 °C (dashed) [Vds = 2.0 V].

Results

Typical current-voltage characteristics at 25°C and 100°C for a 2µm gate length 3D-SMODFET is shown in Fig.(s) 3 and 4, with limited degradation at 100 °C. An effective barrier height > 1 eV extracted from an activation energy measurement is shown in Fig. 5. The low current (< 400 mA/mm) in the device is due to surface depletion in the linear regions around the gate between the source and drain ohmic contacts. A change in the processing sequence has resulted in drain

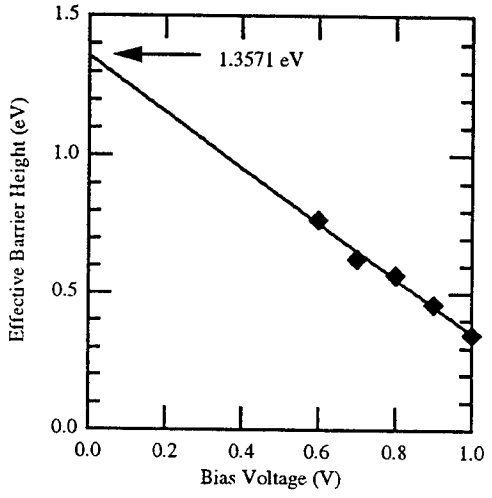

Figure 5 Effective barrier height (eV) for $Al_{.6}In_{.4}As/In_{.65}Ga_{.35}As/$ $Al_{.6}In_{.4}As$ 3D-SMODFET on InP.

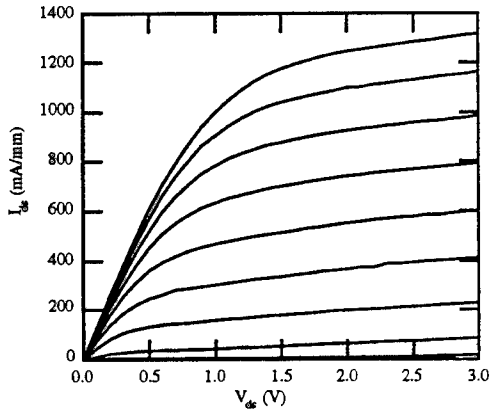

Figure 8 Current voltage (I_{ds} vs. V_{ds}) characteristics of an $Al_{0.6}In_{0.4}As/In_{0.65}Ga_{0.35}As/Al_{0.6}In_{0.4}As$ 3D-SMODFET on InP with a parabolically graded channel [V_{gs} = 0.0 (top), to -2.0 (bottom), 0.25 V steps].

currents > 1000 mA/mm and a DC transconductance of > 500 mS/mm as shown in Fig(s). 8 and 9. The devices have good pinch-off characteristics (< 2.5 V), output conductance (< 15 mS/mm), gate-drain breakdown (2.5 to 7 V) and good microwave performance with a high f_{MAX} to f_T ratio (330/110) for a 0.18 μm gate length.

Discussion

The high temperature performance of a narrow channel $Al_{0.6}In_{0.4}As/ In_{0.65}Ga_{0.35}As/ Al_{0.6}In_{0.4}As$ 3D-SMODFET with record sheet densities (8.5 x 10^{12} cm^{-2}) were shown. The devices have saturation currents of > 1000 mA/mm, gm of > 500 S/mm, good pinch-off characteristics (< 2.5 V), output conductance (<15 mS/mm), gate-drain breakdown (7 V) and good microwave performance with a high f_{MAX} to f_T ratio (330/110).

Acknowledgment

The authors would like to acknowledge the support of William Vanmeerbeke who helped obtain the temperature data and all members of the III-V semiconductor group at Cornell University for valuable discussions. We also acknowledge financial support from QED, Hughes and the ARMY research laboratories (DAAL01-92-C-0266: Project # GC-92-2573).

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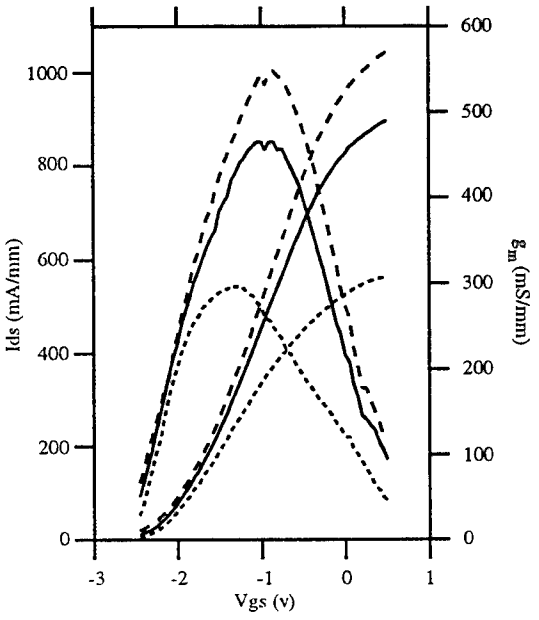

Figure 9 Current voltage (I_{ds} vs. V_{gs}) characteristics of an $Al_{0.6}In_{0.4}As/ In_{0.65}Ga_{0.35}As/Al_{0.6}In_{0.4}As$ 3D-SMODFET on InP with a parabolically graded channel [V_{ds} = 0.5 V (dots), 1.0 V (solid), 1.5 V (dashed)].

Microwave and Millimeter Wave On-wafer Transistor Characterization Capabilities and HFET CAD Model Extraction Techniques

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Abstract

In the past five to ten years there has been considerable advancement both in measurement capabilities at microwave and millimeter wave frequencies and in measurement data analysis. This has resulted in considerable improvements in the techniques for direct extraction of accurate CAD based models. S-parameter measurements can now be performed on-wafer up to 120 GHz allowing for the extraction of small signal CAD models valid to millimeter wave frequencies. This has resulted in the realization of high performance, 20 dB gain at 110 GHz, MMICs for millimeter wave system applications. Optimized measurements systems for noise parameter measurement at microwave frequencies have been demonstrated. Combined with improved CAD models these also allow for the accurate extrapolation of noise parameters to millimeter wave frequencies. In the area of non-linear characterization, while confined to microwave frequencies, new sophisticated measurement systems are presently being developed. These systems operate in the time domain, thus allowing for measurement not only of RF input and output power but also the RF input and output voltage and current waveforms. This information is leading both to an improved understanding of non-linear transistor dynamic behavior but also to the extraction of accurate non-linear models.

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Invited Talk

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Microwave and Millimeter Wave On-wafer Transistor Characterization Capabilities and HFET CAD Model Extraction Techniques

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Most of the work reported here was performed at the Fraunhofer Institute for Applied Solid State Physics, Freiburg, Germany. It involved the contribution of many coworkers all of which I would like to acknowledge, in particular, M. Demmler, J. Braunstein, M. Schlechtweg, R. Bosch and W. Reinert.

Abstract

In the past five to ten years there has been considerable advancement both in measurement capabilities at microwave and millimeter wave frequencies and in measurement data analysis. This has resulted in considerable improvements in the techniques for direct extraction of accurate CAD based models. S-parameter measurements can now be performed on-wafer up to 120 GHz allowing for the extraction of small signal CAD models valid to millimeter wave frequencies. This has resulted in the realization of high performance, 20 dB gain at 110 GHz, MMICs for millimeter wave system applications. Optimized measurements systems for noise parameter measurement at microwave frequencies have been demonstrated. Combined with improved CAD models these also allow for the accurate extrapolation of noise parameters to millimeter wave frequencies. In the area of non-linear characterization, while confined to microwave frequencies, new sophisticated measurement systems are presently being developed. These systems operate in the time domain, thus allowing for the measurement not only of RF input and output power but also the RF input and output voltage and current waveforms. This information is leading both to an improved understanding of non-linear transistor dynamic behaviour but also to the extraction of accurate non-linear models. This invited talk will discuss these measurement systems and the appropriated model extraction techniques.

Motivation/Outline

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The aim of this invited talk is to give you a quick review of;

* the advances in measurement capability that have been achieved over the last five years.
* and the associated CAD model extraction techniques that have been developed/perfected

s-parameters
* Key to describing the basic small signal circuit behaviour of a two-port system.

noise-parameters
* Necessary to describing the noise introduced by the two-port system.

non-linear parameters
* It is becoming increasing important to describe the large signal behaviour of a two-port system.

Introduction

In the past five to ten years there has been considerable advancement in on-wafer measurement capabilities at microwave and millimeter wave frequencies both small signal and large signal. The key to characterization of transistors and MMICs is the measurement of their s-parameters, hence, most of this advancement has been in the area of s-parameter measurements. Improved on-wafer measurement capabilities has also resulted in considerable development and or optimization of the techniques for direct extraction of accurate HFET CAD based models not only for s-parameters determination but also for noise parameters. The latter has been possible through the used of a HFET CAD model that couples the determination of the noise parameters to the equivalent circuit model. These advancements have allowed for the realization of millimeter wave MMICs.

At the present time there is increased interest in high power amplifiers and other non-linear systems and so it is becoming increasingly important to measure not only the small signal behaviour of transistors but also their large signal behaviour. This is stimulating the realization of new sophisticated time domain measurement systems along with the development of non-linear model direct extraction techniques.

s-parameter Measurements

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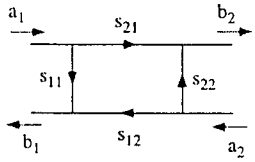
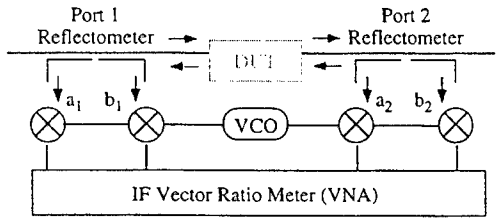


s-parameters
* Key to describing the basic small signal circuit behaviour of a two-port system.

=> "Four Port" Measurement System



Extended to millimeter wave frequencies using two down conversion stages

Measurement Systems: s-parameters

At microwave and millimeter wave frequencies the two-port circuit behaviour of transistors and MMICs is quantified by its four, frequency and bias dependent, s-parameters.

These are generally measured using a "four port" measurement system. This measurement system basically consist of two reflectometers, for example dual directional couples, that allow both the incident and reflected waves to be separately measured. For s-parameter measurement, after appropriate calibration, only the respective ratio's of these parameters need to be measured. This ratio measurement is not performed at the microwave or millimeter wave frequencies but at an IF frequency of a few hundred kHz. The down conversion being performed using mixers or samplers. In commercial systems this approach has been used to produce vector network analyzers (VNA's) that can operate up to 65 GHz.

Millimeter Wave Systems

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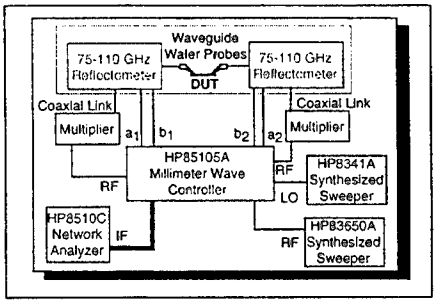
=> Commercial System Available

=> Narrow Band "Waveguide" Measurement Systems 75 GHz to 110 GHz



=> This is a high performance "On-Wafer" Millimeter Wave Measurement System: 70 GHz to 120 GHz

Measurements at higher frequencies can be achieved using two stages of RF down conversion. Using this approach commercial systems are available that can operate up to 110 GHz.

At these frequencies the cable (or waveguide) losses are a major problem degrading the measurement performance of vector network analyzers. By integrating the millimeter-wave reflectometers directly on to the on-wafer probe station this problem can be overcome providing very stable and accurate measurement systems[1]. The system shown, for example, has a raw directivity at the probe tips that is better than -15 dB and can provide for accurate error corrected on-wafer s-parameter measurements from 70 GHz to 118.5 GHz. The biggest source of error in these integrated systems is the quality of the on-wafer calibration standards[2].

1. "A New MODFET Small Signal Circuit Model required for Millimeter-Wave MMIC Design: Extraction and Validation to 120 GHz", P.J. Tasker and J. Braunstein, *Proc. 1995 IEEE MTT-S International Microwave Symposium*, pp. 611-615, Orlando, USA, May 1995.
2. "On-wafer single contact S-parameter measurements to 75 GHz: calibration procedure and measurement system", P.J. Tasker, M. Schlechtweg and J. Braunstein, *Proc. 23rd European Microwave Conference*, 305-307, 1993.

MTA Based Systems

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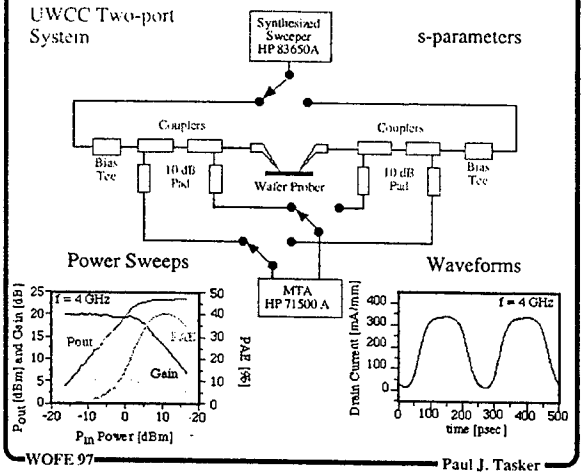
These systems provide for both;

* Frequency Domain Measurements

and

* Time Domain Measurements



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These new large signal measurement systems are based on the HP Microwave Transition Analyzer (MTA)[13]. The MTA is a fully trigger two channel sampling scope with a 40 GHz band width and so operates in the time domain. However, these two channels have a common time base (trigger) allowing, after fourier transformation into the frequency domain, for the measurement of the vector ratio of two waveforms, i.e. s-parameter measurement. As shown in the figure this allow the MTA using an appropriate test-set configuration to provide for vector error corrected swept frequency, fixed power, small signal s-parameter measurements and swept power, fixed frequency, large signal power measurements. The key addition here is that these power measurements are i) performed in the time domian, hence both the harmonic magnitude and phase are measured, and ii) fully vector correct thus giving the actual voltage and current waveforms presents at the measurement plane. In an on-wafer measurement system this is the transistor input and output terminals.

13. "A Vector Corrected High Power On-Wafer Measurement System with a frequency range for the higher harmonics up to 40 GHz" M. Demmler, P. J. Tasker and M. Schlechtweg, *Proc. 24th European Microwave Conference*, pp 1367-1372, Cannes, France, Sept. 1994.

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Transfer Chaarcteristics

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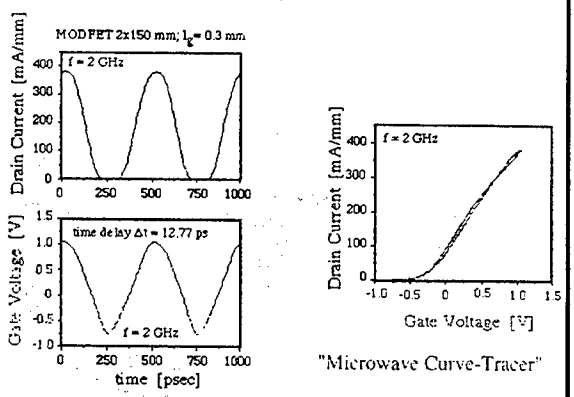
=> Analysis of measured waveforms allows for the direct extraction of dynamic non-linear characteristics



"Microwave Curve-Tracer"

Measurement of the Dynamic RF Transfer Characteristic

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The ability to measure the voltage and current waveforms at microwave frequencies allows for the development of analysis techniques that lead to the direct extraction of the transistor non-linear parameters directly from large signal microwave measurements.

For example, consider the direct measurement of the transistor transfer characteristic from the microwave measurements[14]. This can be simply achieved if the output current waveform is plotted versus the input voltage waveform after accounting for the transmission time delay. The measurement system is thus equivalent to the DC curve tracer except that the measurement is not now being performed at kHz frequencies but at microwave GHz frequencies.

14. "Novel Approach to the Extraction of Transistor Parameters from Large Signal Measurements," P. J. Tasker, M. Demmler, M. Schlechtweg, and M. F. Barciela, *24th European Microwave Conference*, pp. 1301-1306, Cannes, France, Sept 1994.

Slide 18

RF I/V's

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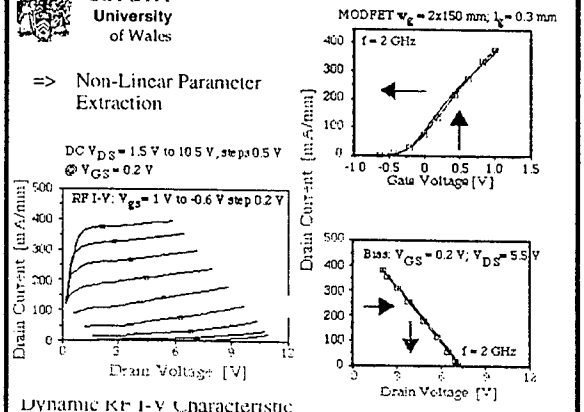
=> Non-Linear Parameter Extraction



Dynamic RF I-V Characteristic

=> In the near future there will be considerable improvement in non-linear parameter extraction techniques based on large signal microwave waveform measurements.

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In addition to the transfer characteristic, by plotting the output current waveform verus the output voltage current waveforms, the dynamic output load line trajectory is also determined. By combining, for example, information determined from these two characteristics it is possible to determine points on the transistors dynamic I-V output characteristic. If these large signal microwave power measurements are repeated for a number of different initial DC bias points the dynamic I-V characteristic can be extracted[14,15].

Non-linear parameters can be extracted from this data in a similar manner to thise developed for the analysis of DC I-V data[15]. This approach can be used to determine the RF breakdown voltage, RF knee voltage, maximum dynamic current swing, hence optimum load impedance. As analysis concepts are further developed[16] its should be possible to extract all four state functions from large signal waveform measurements.

15. "The Determination of the Transistor Dynamic I-V Characteristics from Large Signal Measurements", *Proc. 25th European Microwave Conference*, M. Demmler, P.J. Tasker, J.G. Leckey and M. Schlechtweg, Italy, Sept 1995.
16. "Direct extraction of non-linear intrinsic transistor behaviour from large signal waveform measurement data", M. Demmler, P.J. Tasker, M. Schlechtweg and A Hülsmann, *Proc. 26th European Microwave Conference*, Prague, Sept 1996

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Summary

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=> In the last few years their have been exciting developments in both measurement systems and CAD model extraction techniques.

s-parameters

* millimeter wave measurement systems are now becoming well established
* allows for the development of broadband CAD small signal HFET circuit models
* allows for the development and characterization of millimeter wave MMICs

noise-parameters

* millimeter wave systems are very difficult to realize
* linking noise parameters to the small signal circuit model using the noise temperature model allows for scaling and extrapolation of noise parameters.

non-linear parameters

* Addition of phase information to large signal harmonic measurements allows for determination of waveforms

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Summary

Over the past five to ten years there are been considerable advances in microwave and millimeter wave measurement capabilities. On-wafer measurement of s-parameters to 110 GHz is now almost considered routine. This increased measurement bandwidth has allowed for the determine of the correct physically valid circuit topology that can provides for the accurate scaleable modeling of the measured HFET s-parameters to millimeter wave frequencies.

Combining this HFET circuit model with the noise temperature noise model allows for the extrapolation of HFET noise parameters to millimeter wave frequencies where their direct measurement would be extremely difficult. In addition a simplified noise parameter measurement system has been demonstrated based on this CAD modeling approach.

The present focus is on the development of more advanced large signal measurement systems for the determination of the transistor non-linear parameters. Non-linear parameters extraction techniques based on large signal waveform measurements systems have already been demonstrated.

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Extrapolation

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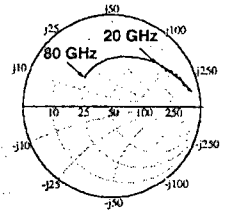
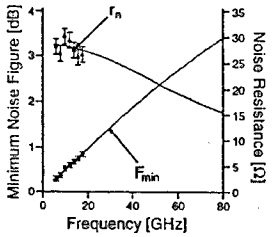
- This CAD noise model allows for simple extrapolation of noise parameters to millimeter wave frequencies for low noise MMIC design





- Noise parameters are equated in terms of a frequency independent parameter T_d (Measured at microwave frequencies)
- Frequency dependence of noise parameters is given by the small signal equivalent circuit model which has been validated up to mm-wave frequencies

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This integrated measurement system which operated over the frequency band from 6 to 18 GHz has been used to determine the noise parameters for millimeter wave frequencies. The noise temperature T_d is determined from these microwave measurements, however, since this parameter is frequency independent the noise parameters at millimeter wave frequencies are determined directly from the circuit model which has been validated upto 120 GHz.

Measured and simulated noise figure of millimeter wave MMICs using this approach were within 0.2 dB at 50 GHz[10]. Also this model can be used to provide for scaling of the noise parameters which enabled both circuit topology and performance optimization of a 12 GHz MMIC[11].

10. "Design and Characterization of High Performance 60 GHz Pseudomorphic MODFET LNAs in CPW-technology based on accurate S-parameter and Noise Models", M. Schlechtweg, W. Reinert, P.J. Tasker, R. Bosch, J. Braunstein, A. Hulsmann and K. Köhler, *IEEE Trans. MTT*, 1992.
11. "Lumped element 12 GHz LNA MMIC using InGaAS/AlGaAs MODFETs with optimized gate width and reactive feedback", R. Bosch, P.J. Tasker, M. Schlechtweg, J. Braunstein and W. Reinert, *Electronic Letters*, 29(15), 1394-1395, 1993

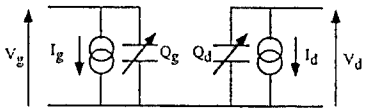
Slide 13

Non-Linear Characterization

Cardiff University of Wales

Key here is that the small signal circuit model is bias dependent.

Under large signal excitation the non-linear bias dependence of these parameters must be accounted for; Model using Four Intrinsic State Functions (I_g, I_d, Q_g and Q_d) in terms of two controlling voltages (V_g and V_d)



- Modeling Options
  - Analytical Solution
    - Limited Parameter Set
    - *Device Specific*
    - *Parameter Extraction*
  - Look-up Table
    - *Complex Parameter Set*
    - Device Independent

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Measurement Systems: non-linear parameters

The small signal models determined from s-parameters measurements are, however, bias dependent. This is not a problem for MMIC receiver applications involving small signals, however, their is an increasing need for MMIC transmitters where large signal are present at the transistor terminals.

In order to accurate design these high power MMICs the non-linear effects caused by the bias dependence of the s-parameters must also be taken into account. Non-linear CAD circuit models are required. Basically this involved modeling the terminal current behaviour of the transistor by four state functions that are controlled by the two terminal voltages. The circuit representation thus involves an input and output circuit consisting off a non-linear current generator in parallel with a non-linear capacitor.

Non-linear parameters are thus required to model the non-linear behaviour of these circuit elements. These non-linear parameters can either be the coefficients of an analytical function that "curve fit" the measured non-linear behaviour (analytical models) or are the measured non-linear behaviour directly (look-up table models).

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Non-Linear Measurements

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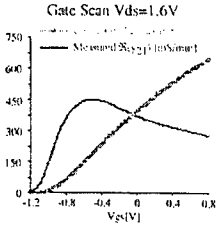
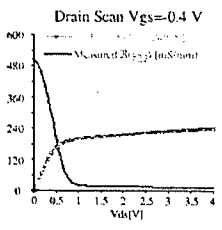
INDIRECT MEASUREMENTS

- Small Signal Parameters → Large Signal Parameters
  "Quasi-Static Solution"
  - → Parameter Extraction
  - → Integrate to get the FOUR State Functions





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Independent of the modeling approach the major problem is the measurement of the non-linear behaviour.

At microwave frequencies this is generally done indirectly. The non-linear behaviour is actually determined by considering the bias dependent small signal s-parameters. This is most apparent in the case of the look-up table model where the integration of the bias dependence small signal s-parameters, after conversion to the respective y-parameters, is used to determine the four state functions directly[12]. However, this also effectively the case in analytical models. In this case the non-linear parameters, function coefficients, are determined by "curve fitting" the derivatives of the analytical function to measured bias dependent small signal s-parameters; i.e. the measured derivatives.

The problem with this indirect approaches is that, i) its assume a quasi-static solution and ii) dispersion effects caused by thermal effects and traps will introduce errors and uncertainties in to the determination of the noise parameters.

12. D. E. Root, S. Fan, J. Meyer, "Technology Independent Large-Signal FETs Models: A Measurement-Based Approach to Active Device Modeling," 1991, Proc. 15th ARMMS Conference

Non-Linear Measurements

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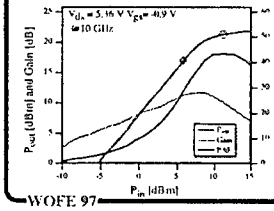
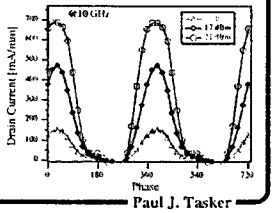
DIRECT MEASUREMENTS

- Large Signal Parameters
  - → Parameter Extraction
  - Thermal Issues
  - Directly Related to MMIC Design
    - → *Parameter Extraction*
- Large Signal Performance
  - Model Verification





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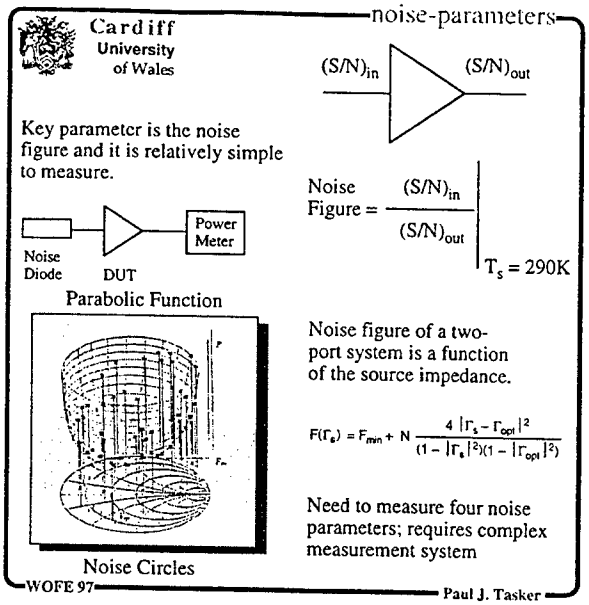
Ideally it would be more accurate if the non-linear parameters where measured directly. The measurement of the DC I-V characteristic is an example of the direct measurement of the transistor non-linear behaviour. Unfortunately, because of thermal effects and traps the dynamic I-V characteristics at microwave frequencies can differ from the DC I-V characteristics. Some of these problems can be resolved by performing pulsed I-V measurements. Even if this measurement could resolve all these issues only two of the four state variables have been measured using these techniques, i.e. the two current generators.

Large signal icrowave measurements are required to directly determine the other two state functions, i.e. the two non-linear capacitors. However, most conventinal large signal microwave measurement systems cannot be used in the direct determine of the non-linear parameters. For example, scalar power compression and harmonic generation measurement systems can only be used for model verification while the more complex load-pull measurements systems can only be used for the direct determine of some of the required MMIC design parameters.

At present a new generation of microwave systems are being developed, however, that enable the direct measuremet of the voltage waveforms at the transistor terminals, hence, allowing for the possibility of direct extraction of all the noise parameter from measured microwave data.

Slide 16

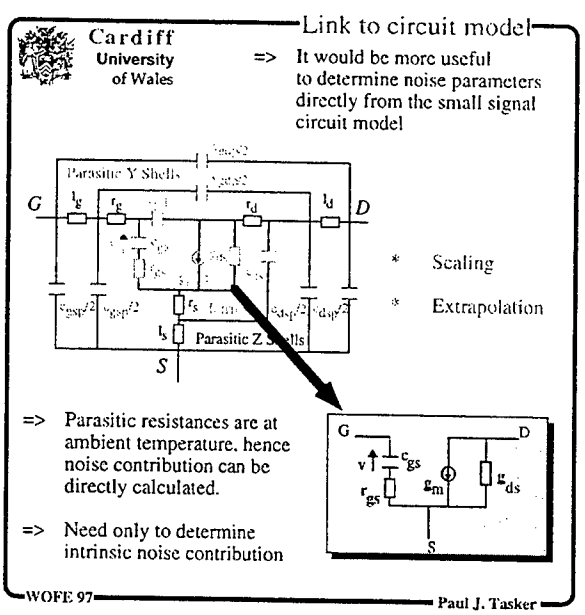


Measurement Systems: noise parameters

Transistors also introduce noise as well as amplifying the input signal, hence degrading the signal to noise ratio. This effect is very important in receiver applications where the input signal can be very weak, for example in the reception of TV or communication signals from satellite transmitters. This effect must be modeled and accounted for in the design of receivers.

The Noise Figure quantifies the change in signal to noise ratio. It can be measured simply by using a variable temperature noise source and a narrow band power meter. Noise figure measurements can thus be performed up to millimeter waves frequencies. However, the noise figure of a two port circuit is also a function of the source impedance. To fully model the noise behaviour of the transistor four noise parameters must be measured. F_{min} the minimum noise figure, R_{opt} and X_{opt} the optimum source impedance that provides the minimum noise figure and N which quantifies the change of the noise figure that results from a change in source impedance.

Slide 9

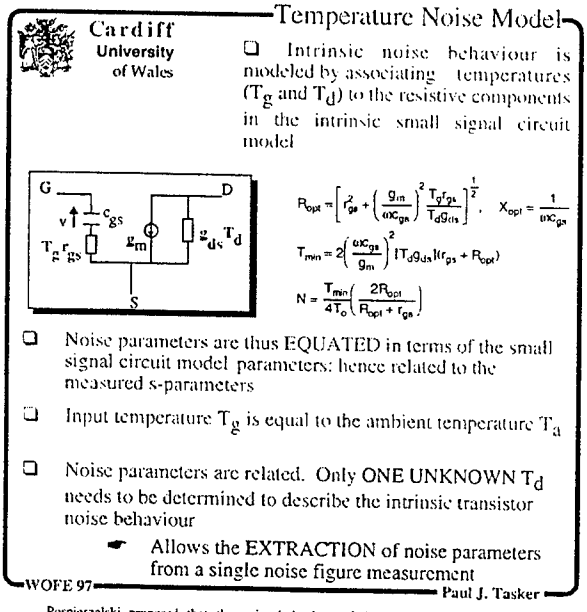


The measurement of the four noise parameters requires a complex measurement system that can vary the source impedance while performing noise figure measurements. The noise parameters are then determined using non-linear "curve fitting" techniques. Commercial noise parameter measurement systems are available only at microwave frequencies, less than 40 GHz.

Determination of the noise parameters independently from the s-parameters is however very limiting. Scaling rules are not well defined and it is also very difficult to extrapolate these parameters to high frequencies. In addition, measurement systems at millimeter wave frequencies have not been developed, hence the design of millimeter wave MMICs requires the accurate extrapolation of the measured microwave noise parameters to high frequencies.

It would be more useful to determine the noise parameters directly from the equivalent small signal circuit model where both scaling rules and accurate extrapolation is possible. The noise contribution of the parasitic circuit is easy to quantify since is results from resistors which simply introduce thermal noise. Thus only a model to account for the noise behaviour of the instrinsic circuit is required.

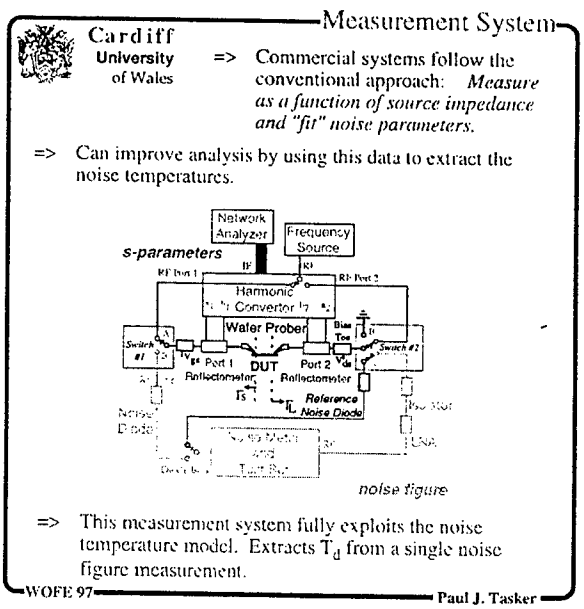
Slide 10



Pospieszalski proposed that the noise behaviour of the transistor could be modeled by associating non-ambient temperatures T_g and T_d to the input resistance r_{gs} and output conductance g_{ds} of the intrinsic circuit model[7] respectively. The noise parameters thus determined in terms of these temperatures and the equivalent circuit element values. Since these temperatures are both gate width and frequency independent this model provides for the determination of noise parameters in a manner that is both scaleable with gate width and can be extrapolated to high frequencies.

In addition, experimental work perfomed by Pospieszalski indicated that the input (gate) temperatures T_g was in fact also equal to the ambient temperature. If this is the case, once the intrinsic circuit element values have been extracted from the measured s-parameters, then only one unknown T_d needs to be determined in order to calculate all four noise parameters. This offers the possibility of extracting of all four noise parameters from a single noise figure measurement.

7. "Modelling of Noise Parameter of MESFET's and MODFET's and Their Frequency and Temperature Dependence," M. W. Pospieszalski, *IEEE Trans. Microwave Theory Techn.*, vol. MTT-37, pp 1340-1350, Sept. 1989.



This extraction approach has been experimentally investigated and shown to be valid within the bounds of experimental accuracy[8]. This data analysis approach can therefore be performed on experimental data determined using conventional measurement systems to provide a data set that links the determination of the noise parameters directly to the small signal circuit model.

In addition, this result allowed for the development a simple noise parameter measurement system that can provide for the fast and accurate determine of HFET noise parameters[9]. This measurement system requires only the integration of a simple 50 Ω noise figure measurement capability into a conventional s-parameter measurement system. If the two measurement system are integrated in the manner shown in the figure all the measurements necessary to allow for full vector correction of the scaler noise figure measurement are possible.

8. "Direct Extraction of all four Noise Parameters from a single Noise figure Measurement", P.J. Tasker, W. Reinert, J. Braunstein and M. Schlechtweg, *Proceedings of the 22nd European Microwave Conference*, 57, 1992.
9. "Transistor Noise Parameter Extraction Using A 50 Ω Measurement System," P. J. Tasker, W. Reinert, B. Hughes, J. Braunstein, and M. Schlechtweg, *IEEE MTT-S International Microwave Symposium*, Atlanta, GA., p. 1251, 1993.

Slide 12

Broadband Systems

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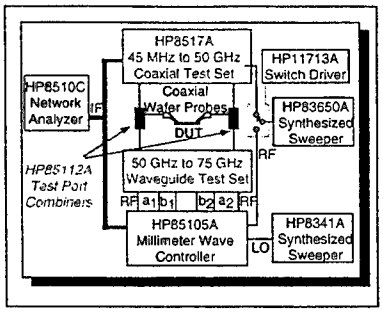
=> For a number of CAD modeling problems Broad Band Systems are required

Approach Employed is to combine two measurement test-sets.



=> This system combines a coaxial 45 MHz to 50 GHz test-set with a waveguide 50 GHz to 75 GHz test-set.

=> Bandwidth of commercial systems based on this approach is continually increasing.

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These millimeter wave measurement systems, however, only cover a single waveguide band. For example, V-band systems 50 to 75 GHz or W-band systems 75 to 110 GHz.

In order to determine accurate small signal CAD circuit models for both passive and active components it is necessary to measure s-parameters over a much broader frequency bandwidth. This can be achieved by measuring the DUT on a number of systems and then combining the measured s-parameters[1]. For on-wafer measurements this introduces an additional error of probe placement repeatability since its involves a number of different probe contacts.

An alternative approach is to combine two test-sets using test-port combiners/diplexers thus allowing for broadband measurement with a single probe contact. The system shown[2], for example, was the first s-parameter measurement system that allowed for broadband measurements up to 80 GHz. This was achieved by combining a 45 MHz to 50 GHz coaxial test-set with a 50 GHz to 75 GHz V-band waveguide test-set.

Slide 5

s-parameter measurement

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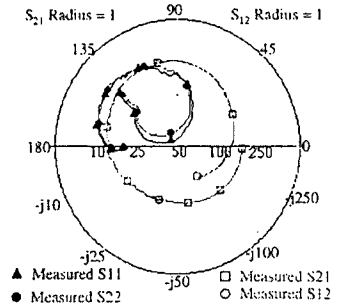
0.5 to 118.5 GHz



Symmetric Passive CPW Structure;
94 GHz 90° hybrid coupler

Continuous measurements across all three bands

s-parameters

* measurement have become established up to millimeter wave frequencies; including on-wafer
* allows characterization of systems at millimeter wave frequencies
* broad measurement bandwidth to aid in the development of small signal CAD models

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Commercial systems are now available that allow for broadband measurements up to 110 GHz by combining a 65 GHz coaxial test-set with a W-band 75 to 110 GHz waveguide test-set. The introduction of the test-port combiner/diplexer, however, does degrade significantly the performance of these systems at millimeter wave frequencies. Single band coaxial systems extending up to 110 GHz are however presently under development.

Further increases in measurement frequency are still possible using this down-conversion four-port approach, however, cable losses between the reflectometers and the measurement plane (probe tips) will considerably limit their accuracy. Active probes provide for a solution to this problem. In this case the measurement system is directly integrated onto the measurement probes. Active probes based on non-linear transmission lines have already been used to perform s-parameter measurements up to 120 GHz[3] and have a potential to reach frequencies approaching 500 GHz.

3. "Full Two-port on-wafer vector network analysis to 120 GHz using Active Probes", R. Yu, M. Reddy, J. Pusl, S. Allen, M. Case and M. Rodwell, *Proc. 1993 IEEE MTT-S International Microwave Symposium*, pp. 1339-1342, Atlanta, USA, June 1993.

Slide 6

Generalized Model

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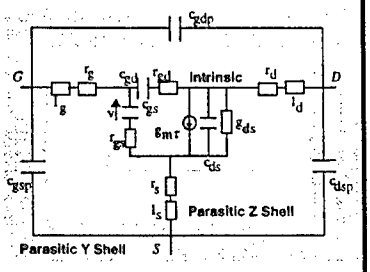
=> Important to accurately model active devices

❑ Generalized Circuit Tolopogy: formulated from series and parallel connections of simple Y- and Z-matrix two-port circuits

❑ Three Shells 17 Circuit Elements is the minimum required to Physically Model Transistors: Scaling and Extrapolation



❑ Only 8 Element values can be determined uniquely at each measurement frequency

❑ "Simple Rule of Thumb" different measurement must be performed for each shell

- Open Test structure or Pinched off "Cold" FET Measurement: Y-Shell
- Short Test Structure of Forward Bias "Cold" FET Measurement: Z-Shell

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While circuits can be designed directly from measured s-parameters it is more common, particularly in the case of active devices, to "fit" the measured s-parameters by an equivalent small signal circuit model. This basically allows for a significant reduction of the data set, however, if the equivalent circuit model is physically valid then the circuit model can be used both for HFET gate width scaling and for extrapolation of the s-parameters to high frequencies. Both features are very important in the design of millimeter wave MMICs[4].

The determination of the equivalent circuit model can be achieved using an optimized "curve fitting" technique. However, this approach will generally determine only the local minimum, hence the solution is a strong function of the initial starting values and is typically not physically valid. If the circuit model determined is to be physically valid it must be directly extracted from measured data[5].

4. "High Performance MMICs in Coplanar Waveguide Technology for Commerical V-Band and W-Band Applications," M. Schlechtweg, W. Reinert, A. Bangert, J. Braunstein, P.J. Tasker, R. Bosch, W. H. Haydl, W. Bronner, A. Hülsmann, K. Köhler, J. Seibel, R. Yu and M. Rodwell, *1994 Microwave and Millimeter-wave Monolithic Circuits Symposium*, San Diego, CA, June 1994.
5. "Bias Dependence of the MODFET Intrinsic Model Element Values at Microwave Frequencies", Brian Hughes and P.J. Tasker, *IEEE Trans. Electron Dev.*, 36 (10), 2267-2273 (Oct. 1989).

Modified Topology

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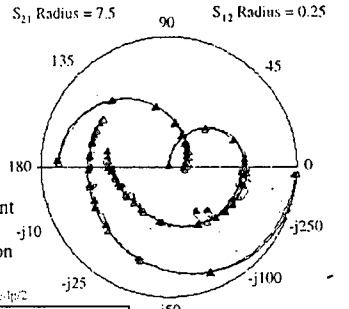
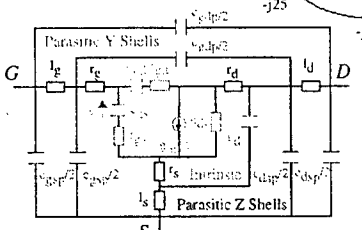


Measured/Modelled S-Parameters from 0.5 GHz to 118.5 GHz

=> Excellent agreement

=> Based on Extraction



Modified Equivalent Circuit Model

=> Broad bandwidth used to perfect circuit Topology

WOFE 97 — Paul J. Tasker

The HFET circuit model is constructed from a parallel and series connection of a number of Y- and Z- matrix circuit shells respectively. The extraction procedures developed to data requires a unique measurement for each circuit shell. The Y-shell is determined from an open circuit test structure[4,5] or the passive "cold" HFET biased into pinch-off[6] s-parameter measurements. The Z-shell is determined from passive "cold" HFET biased s-parameter measurements.

Direct extraction of more than one shell requiring a very large measurement bandwidth in order to measure the high order frequency terms resulting from their interaction. Broadband s-parameters to 120 GHz allowed this to be achieved resulting in a refinement of the HFET equivalent circuit topology[1]. A more distributive circuit topology is required to model the transistor layout parasitics. In addition the measurement data indicated that the transistor output capacitance is mainly associated with the layout, parasitic coupling capacitance, and so should be located outside the parasitic source and drain resistances. This refined topology was able to provide excellent "fit" to the measured s-parameters up to millimeter wave frequencies.

6. "A new method for determining the FET small-signal equivalent circuit", G. Dambrine, A. Cappy, F. Heliodore and E. Playez, *IEEE Trans. MTT*, 36(7), 1151-1159, 1988.

Slide 8

Silicon Nanoelectronics: Prospects and Promises

by

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Abstract

It is widely recognized that the holy grail for nanolectronics is a technology that is compatible with standard silicon. We review the current prospects for the development of such a technology. We will discuss the current prospects for Si based heterojunctions including SiGeC, CaF_2, CeO_2, SiO_2 and ZnS to name just a few. Further, we review the status of one device structures, the tunnel switched diode, which can currently be deployed in a number of applications.

Introduction

It is widely recognized that the current strategy of scaling silicon CMOS will eventually encounter insurmountable challenges. While it is widely discussed exactly where this limit is.generally it is felt that somewhere between 100 nm and 25 nm gate length standard MOS devices will be sufficiently difficult to turn off, that power consumption will become to high.[1] At this point continued shrinkage and hence continuation of the electronics revolution will require a different approach. More than likely this new approach will involve the production of multilayer structures which are electrically active.

Using the standard compound semiconductor approach, one proceeds to search for lattice match semiconductors with the appropriate band offsets. One of the best ways to accomplish this is to examine a McCaldin diagram. In Figure 1, we have a McCaldin of diagram for the lattice constants around Si. From this diagram we can see that the semiconductors that are nearly lattice matched to Si are GaP, AlP and ZnS. The Si/GaP,AlP heterojunction was studied by Kroemer and co-workers.[2] The problems with the growth of GaP on Si due to the difference between polar GaP and the non-polar Si. There has been little effort to develop this heterojunction combination because of the very large number of problems encountered by Kroemer.

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[1] Current Address: VLSI Technologies, San Jose, CA

[2] Current Address: McKinsey and Associates, Dallas, TX

0-7803-4059-0/97/$10.00

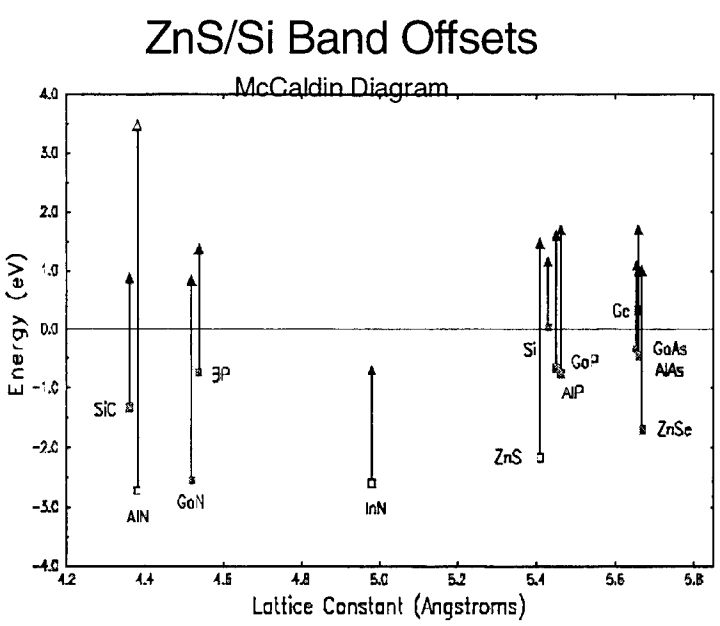

Figure 1. A so-called McCaldin Diagram for Si other semiconductor heterojunctions. The abscissa is energy units with zero of energy being the valence band edge of GaAs. The length of each line is the band gap of the semiconductor and it is positioned to give the valence band and conduction band absolute positions. The ordinate is the lattice constant.

The McCaldin diagram in Figure 1 gives the properties of the ZnS/Si heterojunction. In principle ZnS could act as a barrier layer in a standard heterojunction. This heterojunction has been explored by Kirk and co-workers.[3] The McCaldin diagram indicates that the band offset in the conduction band between Si and ZnS might be rather small. However, recent current voltage measurements on Si/ZnS barrier suggests an acceptable band offset of about 1 eV. The biggest potential problem with this structure is the vastly different growth and processing temperatures for ZnS (<300C) and Si (>500C). However, preliminary results by Kirk and co-workers have demonstrated that novel processing steps maybe employed to produce crystalline Si layers on top of the ZnS barrier layers. Whether or not electrically acceptable layers can be obtained is yet to be determined.

In Table 1, we listed a number of materials that could also be used in making heterojunctions (HJ) with Si. The Si/SiGe heterojunction has been investigated widely. Yet the band offset for the conduction band is rather small making it difficult to fabricate devices such as resonant tunneling diodes (RTD's). Carbon has been added to SiGe to both relieve strain at the Si lattice constant and at the same time perhaps increase the band offset in the conduction band. While the amount of carbon that can be incorporated into SiGe maybe quite small, it maybe enough to produce a substantial band offset.[4] The growth of CaF_2/Si heterojunctions has been studied extensively without any clear success in growing Si on CaF_2.[5] Attempts to grow devices using the Si/SiO_2 combination have

been plagued by the amorphous nature of the layers. The remaining HJ combinations involving Al_2O_3, CeO_2 and PrO_2 are all under investigation for their HJ properties.

An alternative approach has been to fabricate a so called tunnel switched diode which

Table 1. The properties of materials important in looking for Si based heterojunctions

Material	Lattice constant (nm)	Mismatch to Si	Structure
Si	0.54307	0	Diamond
Ge	0.56579	+4.2	Diamond
C	0.35668	-34.3	Diamond
CaF_2	0.54640	+0.6	CaF_2
CeO_2	0.5411	-0.37	CaF_2
PrO_2	0.539	-0.70	CaF_2
Al_2O_3	a=.4758;c=1.2991	5.5/12.3	Hexagonal
SiO_2	N/A	N/A	Amorphous

only involves a single oxide layer on a pn junction. This device gives a S-type negative resistance and could in principle replace many of the heterojunction devices.[6]

The success in finding an adequate replacement for Si based electronics beyond the post shrink era is not assured. Yet the importance of this research area is such that continued search for a replacement is one of the most important activities in modern electronics research.

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[2] Wright, S.L.; Kroemer, H.; Inada, M Journal: Journal of Applied Physics vol.55, no.8 p.2916-27 (1985).
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[4] E. T. Yu, E. T. Croke, A. T. Hunter, to be published.
[5] Pettersson-PO (*R) Miles-RJ McGill-TC JOURNAL OF APPLIED PHYSICS v76 (11) : pp7328-7331 (1994).
[6] Levy, H. J,. Daniel, E. S., and McGill, T. C. "A Transistorless Current Mode Static RAM Architecture - Submitted to .IEEE Journal of Solid State Circuits.

Multiple-Valued Logic Circuits Using Resonant Tunneling Diodes

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1 Introduction

The intent of this poster demonstration is to explain how resonant tunneling diodes (RTDs) can be utilized to design multiple-valued logic (MVL) circuits in a very compact and efficient manner, where the non-linear fold-back characteristic of RTDs provides unique advantages in the realization of specific functions that are central to the design of MVL circuits. At the University of Michigan, a comprehensive effort is being made to demonstrate through simulation, validation and fabrication that RTDs and associated tunneling devices such as BSRTTs, RHETs, RTBTs, etc. can be employed to realize ultra-high-speed and ultra-high-density digital circuits. Here, we show four different types of multi-valued logic circuits consisting of RTDs in conjunction with HBT and CMOS devices: *multivalued gate arrays*, *multivalued 4-step counter*, *multivalued multiplexer*, and *multivalued signed-digit adder*. These designs have been simulated using NDR-SPICE, a circuit simulator that has been developed at the University of Michigan to handle quantum electronic devices, and their at-speed performance has been accurately estimated by using a suite of CAD tools, also developed at the University of Michigan. The circuits have been built at the bread-board level by using discrete components, and their functionalities were verified. We have then transferred the technical knowhow to Lockheed Martin for monolithic fabrication of the first three MVL circuits.

2 Multivalued Gate Arrays

Multivalued gate arrays can be employed to implement any arbitrary multivalued Boolean functions by simply programming interconnects. Both one- and two-input four-valued logic gates have been designed, built and tested in our laboratory. Figure 1 illustrates a 4-valued gate array that can be programmed by appropriately mask-selecting the interconnects to realize one of the possible four billion functions of a two-input four-valued logic gate. Resonant-tunneling diodes (RTDs) have been utilized to realize the literal functions that are key to realizing the MVL functions.

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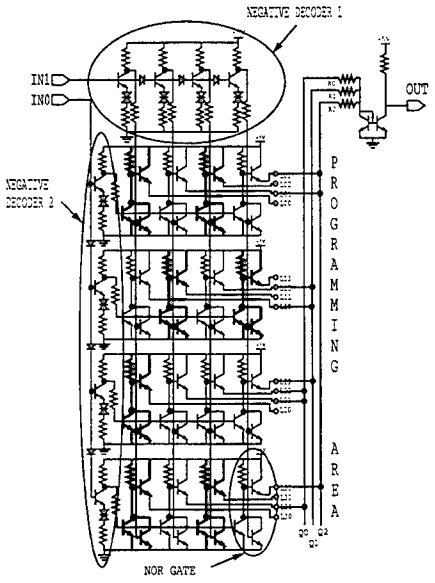

Figure 1: A 2-input 4-valued logic circuit

3 Multivalued Multiplexer/Demultiplexer

Figure 2 illustrates the design of a 4-valued multiplexer (a demultiplexer can be similarly built by slightly modifying the circuit) where the output can select one of the four inputs depending on the multivalued signal inserted into the Select input. As shown in the diagram, the multiplexer can be used both as an analog channel selector, where the RTD ladder circuit can steer analog signals at the data input terminals to the output terminal with minimum amount of cross-channel modulation and signal distortion, or as a 4-valued digital multiplexer (also called T-gates), which can be employed to realize various quaternary Boolean logic operations.

4 Multivalued Counter

Figure 3 shows the design of a 4-valued down counter designed using only 3 transistors and a multiple-peak resonant tunneling diode (MPRTD). This counter can be used to generate the multivalued signal needed to select multiplexers and demultiplexers. A conventional design using CMOS would require at least 30 devices. Our novel circuit technique also offers improved compactness as compared to a multiple-valued counter described by Kuo *et al* that uses one multi-peak RTD and 7 transistors. The counter cycles through four logic levels, determined by the occurrences of RTD peaks, with the clock pulse, from high to low one level at a time. It consumes 210 mW while operating at a speed of 500 MHz.

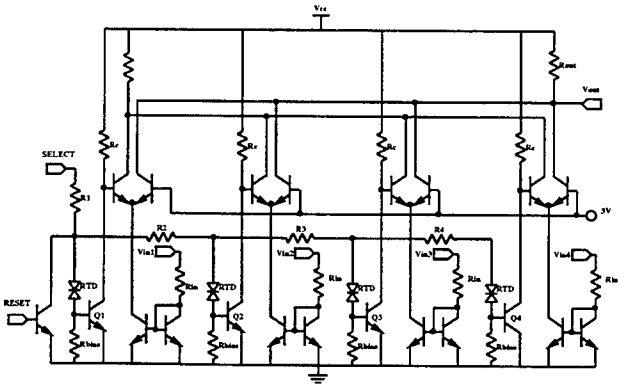

Figure 2: 4-input RTD multiplexer

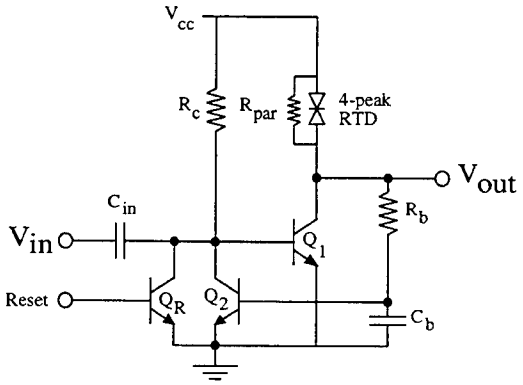

Figure 3: Four-valued down counter

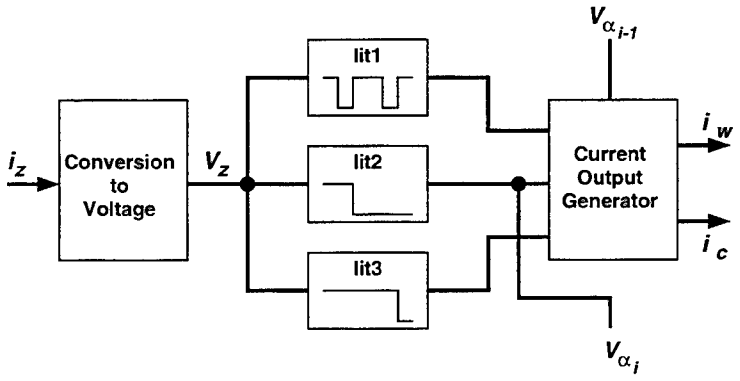

Figure 4: Block diagram of the SDFA cell

5 Multivalued Signed-Digit Adder

A signed-digit adder using a combination of RTD and CMOS devices has been designed. This design, shown in Figure 4, uses *current-mode* signal representation which allows *wired addition* of signals. The adder implements radix-2, signed-digit addition, and hence requires a three-level logic (using digits $\{-1, 0, +1\}$). The adder functions allow realization of addition operations with no carry ripple. This new signed-digit adder uses 13 MOS transistors, while 44 transistors are used in an equivalent redundant-binary static CMOS implementation. The design was verified using a circuit simulation tool, and a prototype was built for demonstrating the functionality. The circuit prototype consists of a CMOS chip, fabricated using a standard 2-micron process, to which RTDs were connected externally. We have also designed, fabricated and tested a prototype 7x7 parallel multiplier in CMOS which uses redundant signed digit arithmetic. The SDFA circuit finds use in embedded computing subsystems such as a fast multiplier for high performance microprocessors.

Future Directions: Theory and Modeling

Magneto-optics of arrays of quantum dots and antidots

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(January 3, 1997)

We study the optical absorption of arrays of quantum dots and antidots in a perpendicular homogeneous magnetic field. The electronic system is described quantum mechanically using a Hartree approximation for the mutual Coulomb interaction of the electrons. The model is particularly suited for the investigation of the far-infrared absorption of gate-modulated systems, where the gate not only controls the distribution of the electrons, but also modulates the external radiation field.

I. INTRODUCTION

The electric transport properties of a two-dimensional electron gas (2DEG) in a lateral superlattice potential have been studied experimentally [1–4] and theoretically [5–11] for some time, to cite just a few contributions. The far-infrared optical properties of these systems [12–18] have not been investigated to the same extent, although the optical properties of independent quantum dots and wires have enjoyed great attention in recent years [19–25].

In this communication we shall describe a model and preliminary results for the far-infrared (FIR) absorption for electrons in a lateral superlattice and a perpendicular magnetic field. The model has been used to shed some light on important questions in fundamental research on the magneto-optics of a 2DEG. Here we shall focus our attention on issues that might proof to be important in the calculation of the optical properties of mesoscopic devices, the role of the Coulomb interaction between the electrons and the modulation of the external electromagnetic field by a gate electrode.

II. MODEL

To describe the electrons in the conduction band in the presence of a lateral superlattice at the AlGaAs-GaAs interface in a constant perpendicular magnetic field $\mathbf{B} = B\hat{\mathbf{z}}$ we employ a model of a 2DEG, with the three-dimensional charge density given by $-en_s(\mathbf{r})\delta(z)$, and $\mathbf{r} = (x, y)$. The square superlattice is spanned by orthogonal lattice vectors of length L, the primitive translations of the Bravais lattice $\mathcal{B}$. The corresponding reciprocal lattice $\mathcal{R}$ is spanned by $\mathbf{G} = G_1\mathbf{g}_1 + G_2\mathbf{g}_2$, with $G_1, G_2 \in Z$, $\mathbf{g}_1 = 2\pi\hat{\mathbf{x}}/L$, and $\mathbf{g}_2 = 2\pi\hat{\mathbf{y}}/L$. The external periodic antidot potential the electrons are moving in is taken to be of the form

$$V(\mathbf{r}) = V_0 \left\{ \sin\left(\frac{g_1 x}{2}\right) \sin\left(\frac{g_2 y}{2}\right) \right\}^2 . \qquad (1)$$

The electron-electron interaction is included in the Hartree approximation (HA) leading to an effective single-electron Hamiltonian $H = H_0 + V_H(\mathbf{r}) + V(\mathbf{r})$, where $V_H(\mathbf{r})$ is the effective potential in a medium with a dielectric constant κ, felt by each electron and caused by the total charge density of the 2DEG, $-en_s(\mathbf{r})$, and the neutralizing background charge density $+en_b = +e\langle n_s(\mathbf{r})\rangle$. We neglect all impurity and phonon effects.

The periodic external potential $V(\mathbf{r})$ and the constant external magnetic field imply that all physical quantities of the noninteracting system are periodic with respect to translations of $\mathbf{R} \in \mathcal{B}$. The periodicity of the Hartree potential follows from that of $n_s(\mathbf{r})$. The commensurability [26] condition between the period length L and the magnetic length $l = (\hbar c/eB)^{1/2}$ requires the magnetic flux through one lattice cell or an extended cell to be an integer pq times the flux quantum $\Phi_0 = (hc/e)$. Each Landau band splits into pq magnetic subbands [27,20].

In the calculations we use the symmetric basis functions constructed by Ferrari [28] and used by Silberbauer [27]. The set of Hartree equations has to be solved iteratively together with the condition that the average electron density $n_s = N_s/A$ is constant, which determines the chemical potential μ. N_s is the number of electrons per unit cell with area A in $\mathcal{B}$.

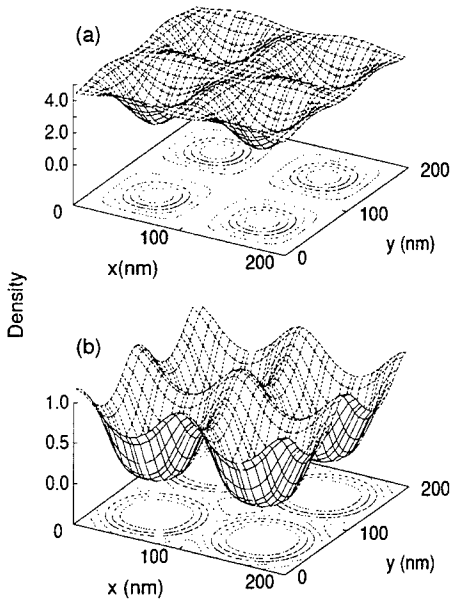

FIG. 1. The two-dimensional electron density $n_s(\mathbf{r})$ in a lattice of antidots for (a) $N_s = 4.0$ and (b) $N_s = 0.5$. $L = 100$ nm, $pq = 4$, $B = 1.65$ T, $l = 19.9$ nm, $V_0 = 5.0$ meV, $T = 1.0$ K, $m^* = 0.067m_e$, and $\kappa = 12.4$.

The density $n_s(\mathbf{r})$ in four unit cells of the interacting 2DEG is shown in Fig. 1 for the case of one Landau band filled (a) or only one subband filled (b). For low N_s the electrons tend to gather in the space between four antidots, but in the case of one Landau band filled the density forms almost flat regions everywhere between the antidots. This is the precursor for the formation of an incompressible region between the antidots in a larger system.

In order to calculate the FIR absorption of the 2DEG we perturb it by a monochromatic external electric field without restricting it's dispersion relation to that of a free propagating field. The power absorption $P(\hbar\omega, \mathbf{k})$ is calculated from the Joule heating of the self-consistent electric field consisting of the external and the induced field [16]. The peaks in the absorption spectra represent absorption of the collective modes of the 2DEG. Single-electron excitations are strongly damped and do not show up in the spectra [16]. The power dissipation is made possible by retaining a small but finite imaginary part of the frequency in the electron susceptibility.

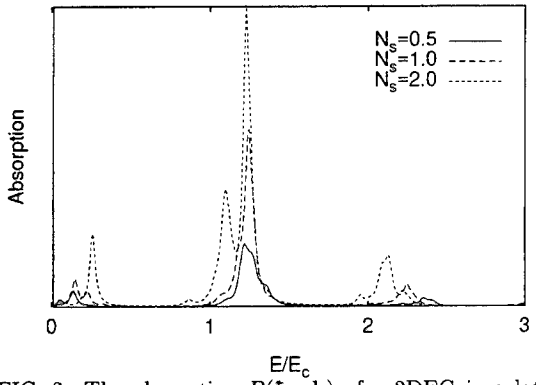

FIG. 2. The absorption $P(\hbar\omega, \mathbf{k})$ of a 2DEG in a lattice of antidots for three values of N_s, $\mathbf{k}L = (0.2, 0)$ $E_c = \hbar\omega_c$. Other parameters are as in Fig. 1.

III. RESULTS

The absorption of the 2DEG in an antidot lattice with GaAs parameters, $m^* = 0.067m_e$ and $\kappa = 12.4$, is shown in Fig. 2 for a monochromatic electric field with $\mathbf{k}L = (0.2, 0)$. For small wave vectors $P(\hbar\omega, \mathbf{k})$ is almost independent of $\mathbf{k}$. We find the two main absorption peaks predicted by semiclassical models [17], ω_+ just above the cyclotron frequency $\omega_c = eB/(m^*c)$, and the low frequency ω_- peak well below ω_c. The antidot potential (1) does not imply any generalized Kohn's theorem [19,29], blocking absorption caused by an internal motion of the 2DEG, so we observe an absorption peak just above $2\omega_c$.

The energy dispersion of the "single-electron" Hartree Landau bands along the diagonal of the first magnetic Brillouin zone is shown in Fig. 3 for the lowest band only partially occupied (a), or completely occupied (b).

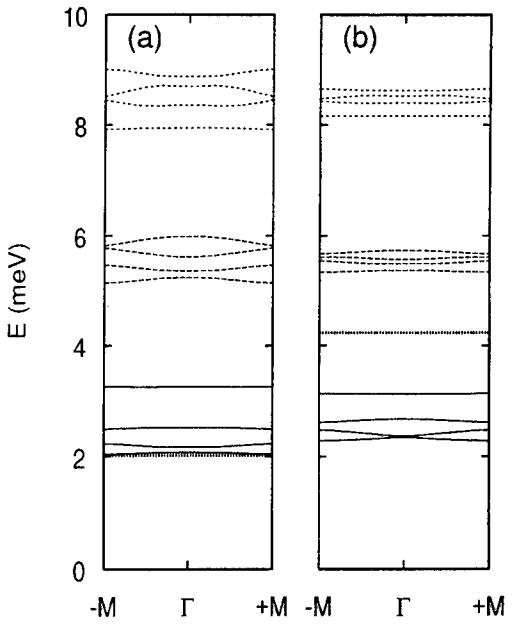

FIG. 3. The Hartee energy spectrum along the diagonal $-M \leftrightarrow \Gamma \leftrightarrow +M$ in the first magnetic Brillouin zone for a 2DEG in a lattice of antidots for two choices of N_s. The chemical potential μ is indicated by a horizontal line. Other parameters are as in Fig. 1.

The absorption peaks in Fig. 2 do not correspond directly to single-electron transitions but represent absorption caused by collective oscillations of the 2DEG. The peak just above $2\omega_c$ can thus be identified through the induced density to be caused by the excitation of a harmonic of the fundamental magnetoplasmon. The low energy peak represents an edge magnetoplasmon around each antidot according to the semiclassical model at a high magnetic field. How closely these classical or semiclassical ideas can be used to describe the motion of the 2DEG in a system with small lattice lengths is still under investigation.

The electron-electron interaction "mixes" the single-electron states in the ground state making the width of the Landau bands dependent on N_s and breaking possible selection rules for the absorption. The shift of the absorption peaks in Fig. 2 does not only result from the motion of the chemical potential μ as a function of N_s but is also caused by the dependence of the effective interaction $V_H(\mathbf{r})$ on N_s, and thus the changing subband structure. It is therefore essential to include the interaction in the ground state calculation in order to get correct location and oscillator strength of the absorption peaks. An example of this is shown in Fig. 4, where the self-consistent absorption is compared to the absorption for a 2DEG without including the interaction in the ground state calculation. The interaction in the ground state and

the excited state are not treated on the same basis violating general conservation laws as the Ward-Takahashi identity [30].

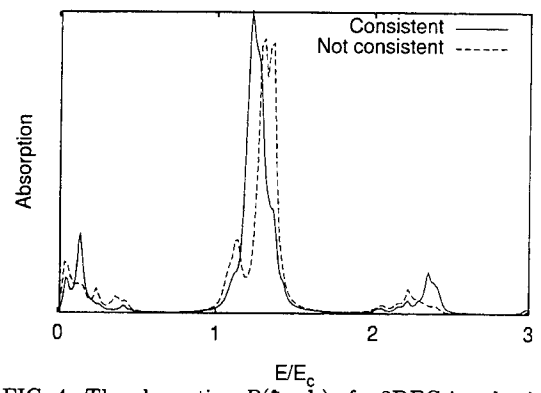

FIG. 4. The absorption $P(\hbar\omega, \mathbf{k})$ of a 2DEG in a lattice of antidots calculated self-consistently with interaction effects in ground state and excited state compared to an inconsistent use of a non-interacting ground state. $\mathbf{k}L = (0.2, 0)$, $N_s = 0.5$, $pq = 4$, $E_c = \hbar\omega_c$. Other parameters are as in Fig. 1.

The effects of not performing the calculation totally self-consistently within a certain approximation, as the HA, can in some cases be minimal or large in other cases, but they are usually not easily predictable without a calculation.

Here we have assumed the external electric field to have a finite but small wave vector $\mathbf{k}L = (0.2, 0)$. Ordinary far-infrared light would have a much smaller wave vector so we have justified this choice with the fact that the absorption is rather insensitive to a small $\mathbf{k}L$, even though this value would be enough to break Kohn's theorem in the absorption of a homogeneous 2DEG [16] or electrons parabolically confined to a quantum dot [21]. The sample we are modelling here has a metal gate on top that is modulated in order to create the antidot potential (1). The gate not only modulates the static potential the 2DEG feels but also affects the time-dependent external electric field. In order to investigate the lowest order effects of this modulation we have calculated the absorption for a monochromatic electric field with a wave vector corresponding to a simple inverse lattice vector parallel to the antidot lattice, $\mathbf{k}L = (0.2 + g_1 L, 0)$, or diagonal to the lattice, $\mathbf{k}L = (0.2 + g_1 L, g_2 L)$. The results are seen in Fig. 5.

The absorption of an electric field modulated with a vector of the inverse lattice still has a peak coinciding with the peak at ω_+, but in addition it has a parallel peak for a bit higher energy. This is in accordance with the semiclassical model [17], but the finer details may differ due to interaction effects reflected by the screening properties of the 2DEG, that are neglected in the model. The Landau band structure plays an important role in the fully quantum mechanical calculation introducing higher order harmonics of the fundamental absorption peaks above each multiple of the cyclotron frequency ω_c.

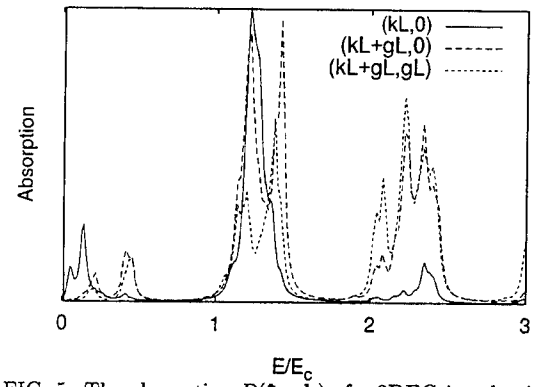

FIG. 5. The absorption $P(\hbar\omega, \mathbf{k})$ of a 2DEG in a lattice of antidots for three choices of the wave vector $\mathbf{k}$: $\mathbf{k}L = (0.2, 0)$, $\mathbf{k}L = (0.2 + g_1 L, 0)$, and $\mathbf{k}L = (0.2 + g_1 L, g_2 L)$. $E_c = \hbar\omega_c$. Other parameters are as in Fig. 1.

Clearly, the shorter modulation considerably enhances the oscillator strength of higher order magnetoplasmons, and the polarization diagonal to the antidot lattice markedly reduces the relative strength of the fundamental plasmon. Similar effects are observed in calculations for a lattice of coupled quantum dots, not only the deviation of the confinement potential from a parabolic shape activates internal motion of the 2DEG in individual quantum dots, but also the strong periodic modulation of the external time dependent electric field excites internal motion in addition to the center of mass motion predicted by the generalized Kohn's theorem. Presently, the absorption is calculated self-consistently in exactly two-dimensions. To correctly account for the effects of the gate electrode on the absorption the third dimension, along the growth direction, has to be incorporated into the model self-consistently. Until now we have not considered this feasible due to the size and time requirements on the computing resources caused by the presence of the magnetic field and the self-consistency requirement. The modulated gate is commonly used as a grading coupler, even in structures with a homogeneous 2DEG, to couple the electromagnetic field and the 2DEG at a certain finite wave vector [31,32,15].

IV. SUMMARY

We have here presented a fully quantum mechanical model of the far-infrared absorption of a 2DEG in a lateral superlattice of antidots. The calculations have been carried out self-consistently within the HA for the ground state properties. This self-consistency is paralleled by the usage of the time-dependent HA for the excited state [33]. We treat the interaction between electrons within one unit cell of $\mathcal{B}$ in the same manner as the interaction

between electrons of different unit cells. The strict observance of the periodicity of the system requires that we fulfill the commensurabilty condition between the magnetic and the period length. This complicates the calculation and can increase both the computer size and CPU-time needed in a numerical calculation when we want to repeat calculations for different values of the magnetic field B. A calculation of the dispersion of the absorption as a function of B is therefore very time consuming, but the variation of the electron density is easy to handle. On the other hand we are free to consider almost any type of a periodic potential, we can thus study the transition from a system of quantum dots to a system of antidots by increasing the number of electrons per unit cell.

The presence of the perpendicular magnetic field allows us to study many interesting problems of basic research, such as the formation of incompressible regions in the density and their effects on the absorption, or the formation of Bernstein modes [34,20]. The absence of a magnetic field would make the calculation of the absorption much simpler, but the effects of the electron-electron interaction and the metal gate of the heterostructure would be of same importance for a 2DEG in a periodic potential of antidots.

ACKNOWLEDGMENTS

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FET MODELING FOR ANALOG AND DIGITAL APPLICATIONS

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Abstract: We consider some recent developments in the modeling of submicrometer field effect transistor devices for use in design of analog and mixed mode applications. We emphasize the use of unified models with a precise and continuous description of the *I–V* and *C–V* characteristics in all regimes of operation, including the transition regions. The models incorporate short-channel and high-field effects, gate leakage current, and temperature dependencies of device parameters.

Introduction

The scaling of FET feature size into the deep submicron range, and the recent strong emphasis on high-speed, low-power and low-noise mixed-mode digital and analog applications, has necessitated the development of new, enhanced device models for use in circuit simulators such as SPICE[1]. These *I–V* and *C–V* models emphasize a high degree of precision and the use of continuous, unified and analytical expressions through all regimes of operation—saturation, triode, near-threshold, and subthreshold. The models should also include the short-channel and high-field mechanisms characteristic of down-scaled FETs, such as drain-induced barrier lowering (DIBL), channel length modulation (CLM), and phenomena related to hot electron induced impact ionization (degradation, substrate current, kink effect, and breakdown).

Additional modeling challenges in FETs are: gate leakage (HFET, MESFET), temperature dependence and self-heating (HFET, MESFET, SOI/MOSFET), side- and back-gating (HFET, MESFET), frequency dependence of model parameters, scaling of model parameters, and the increasing relative importance of parasitics with down-scaling.

Our new, enhanced FET models, suitable for simulation of mixed mode circuits, incorporate the following features:

* Modeling of sub-0.1 μm MOSFETs
* Modeling of GaAs MESFETs accounting for gate leakage current and frequency dispersion.
* Modeling of *n*- and *p*-channel HFETs, needed for simulation of complementary HFET digital circuits (C-HFET).
* Modeling of the subthreshold leakage, needed for the modeling of standby power consumption in digital circuits.
* Modeling of the near-threshold operation, needed for the modeling of low-power operation.
* Accurate description of differential, benchmark quantities such as g_m/I_d and g_d, by inclusion of effects such as DIBL, CLM and frequency dependent parameters.

Modeling Approach

Our FET models are based on a description of the density of charge carriers in the conducting FET channel given by the unified charge-control model (UCCM)[2]. With this

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approach, all regimes of device operation are covered, including the near-threshold regime, which is very important for FETs with submicron feature size and reduced power supply voltages, especially in low-power operation. UCCM has been shown to work particularly well for FETs with a narrow channel confined to a semiconductor/oxide interface (MOSFET) or a heterointerface (HFET). When adjusted for the presence of a finite thickness of the conducting layer, this model is also applicable for MESFETs[3].

I–V Model

A continuous (unified) model for the FET current-voltage characteristics is obtained by expressing the drain current in each regime of operation—subthreshold, above-threshold linear, and above-threshold saturation—and then joining the various expressions using suitable interpolation functions. The resulting model can be written in a universal form applicable to all types of FETs[2,3]. Most of the essential, device specific features of the model, including a description of the transition to the subthreshold and the saturation regimes, are expressed through the linear channel conductance g_{ch} and the saturation current I_{sat}. The equations for these quantities, which can be derived from UCCM and a simplified velocity-field relationship, also incorporate short-channel and high-field effects.

C–V Model

An accurate model of the intrinsic capacitances associated with the gate region of FETs requires an analysis of the variation of the charge distribution in the channel versus terminal bias voltages. For MOSFETs, the problem is normally simplified by assigning the channel and depletion charges to the various "intrinsic" terminals, a procedure that assures charge conservation. Based on this charge assignment, we can define a set of so-called transcapacitances $C_{ij} = \kappa_{ij}\partial Q_i / \partial V_j$ where $\kappa_{ij} = -1$ for $i \neq j$ and $\kappa_{ij} = 1$ for $i=j$, Q_i are the terminal charges, V_j are the intrinsic terminal voltages, and where the indices i and j run over the terminals. These are similar to the charge-based, non-reciprocal capacitances introduced by Ward and Dutton[4]. In a four-terminal FET, such as the MOSFET, we have a total of 16 transcapacitances of which 9 are independent. In three-terminal FETs, such as HFETs and MESFETs, we have a total of 9 transcapacitances, of which 4 are independent[3]. The equivalent circuit for the three-terminal case is shown in Fig. 1a. A simplified model is obtained by using the so-called Meyer capacitances—the subset of capacitances obtained as derivatives of the intrinsic gate charge[1] (see Fig 1b) Although charge conservation is not strictly enforced by using the Meyer capacitances, the resulting error is usually small, except for especially demanding circuits such a charge pumps and switched capacitor circuits[5].

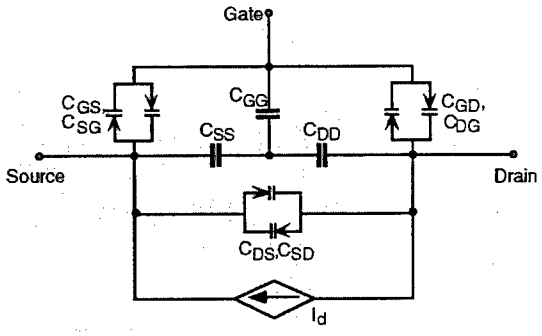

Fig. 1a. Large-signal MESFET and HFET equivalent circuits corresponding to a complete charge based capacitance model. (After Fjeldly et al. [3]).

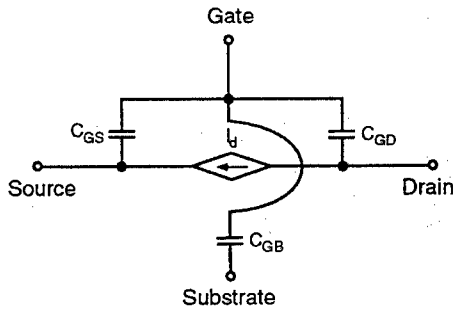

Fig. 1b. Large-signal equivalent circuit of intrinsic MOSFET based on Meyer's capacitance model. (After Fjeldly et al. [3])

Modeling examples

Sub-0.1 μm MOSFET

Fig. 2 shows a comparison of our MOSFET model (AIM-Spice level 7) with experimental *I-V* characteristics for a sub-0.1 μm MOSFET[6]. We observe an excellent agreement in all regimes of operation, including the sub-threshold and near-threshold regimes. Also note the horizontal shift of between the subthreshold transfer characteristics, corresponding to drain-induced barrier lowering. This also gives rise to the slope in the near threshold *I–V* characteristics near threshold of Fig. 2a.

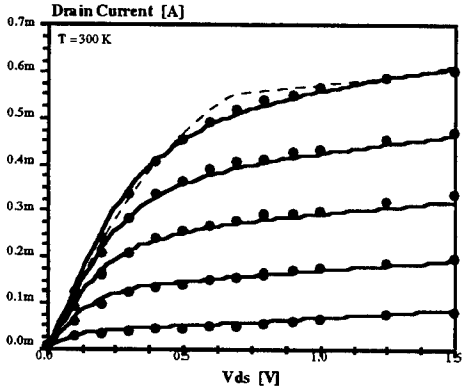

Fig. 2a. Experimental (symbols) and simulated (lines) *I–V* characteristics for a deep submicron nMOSFET with L_{eff} = 0.09 μm. V_{gs} from 0.5 V to 1.5 V in 0.25 V steps. Dashed line is a simulation based on MOSFET level 3 for V_{gs} = 1.5 V. (After Ytterdal et al. [6]).

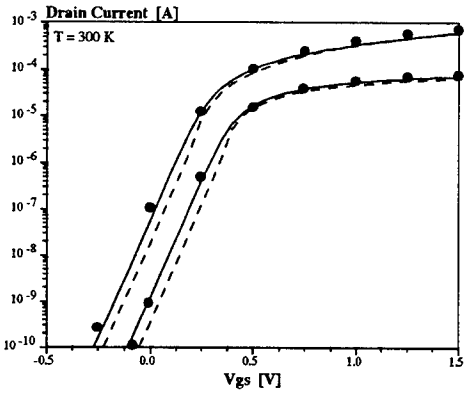

Fig. 2b. Subthreshold experimental (symbols) and simulated (lines) transfer characteristics for the same nMOSFET as in Fig. 2a. Dashed and solid lines are simulated results using level 3 and 7, respectively. V_{ds} = 0.05 V and 1.55 V (After Ytterdal et al. [6]).

MESFET conductances

Fig. 3 verifies that our MESFET model accurately reproduces differential quantities such as the ratio of transconductance and drain current, and the channel conductance[7]. This is very important for an accurate simulation of analog and mixed mode circuits. Our model also includes the temperature dependencies of the important MESFET model parameters.

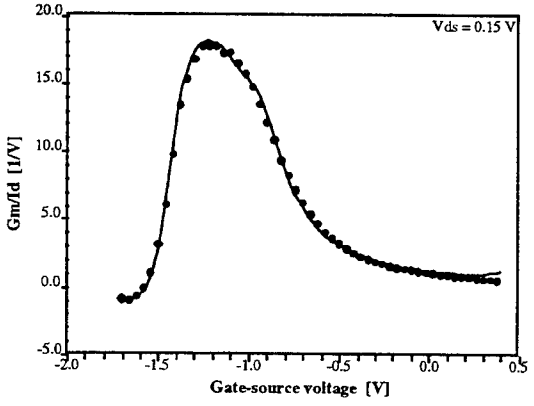

Fig. 3a. Measured (symbols) and modeled (line) ratio of transconductance and drain current versus V_{gs} for a 0.5 μm MESFET. (From Ytterdal et al. [7]).

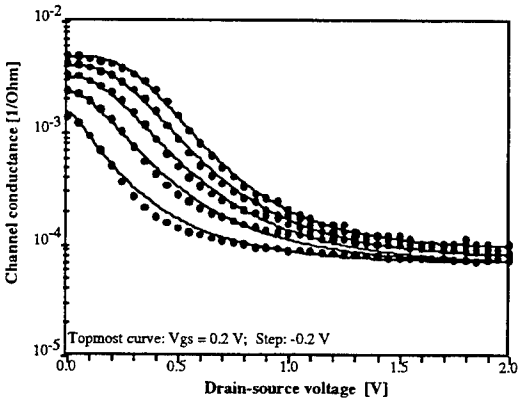

Fig. 3b. Measured (symbols) and modeled (line) channel conductance versus V_{ds} for different V_{gs} . Same device as in Fig. 3a. (From Ytterdal et al. [7])

HFET gate leakage and S-parameters

Our HFET model incorporates a precise model of gate leakage current, including the effects of hot carriers near drain. A comparison with experimental gate current is shown in Fig. 4a. The importance of including frequency dependence of modeling parameters is illustrated in the *S*-parameter plot in Fig. 4b.

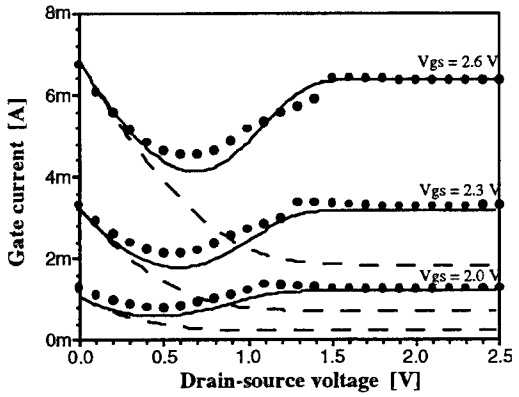

Fig. 4a. Measured (symbols) and simulated gate current versus V_{ds} for a 0.8 μm long, 10 μm wide HFET. Dashed lines corresponds to simulation results with the hot-carrier effect disabled in the model. Data from Lee *et al.* [8].

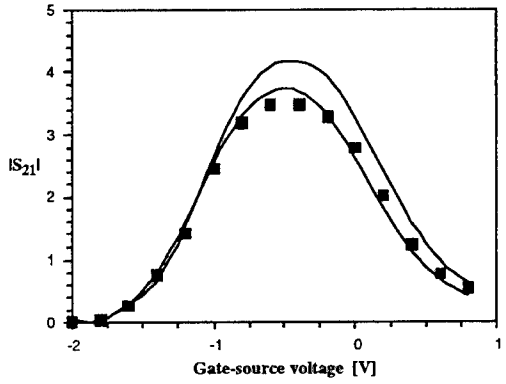

Fig. 4b Measured (symbols) and simulated (solid lines) magnitude of S_{21} versus gate-source voltage at 1 GHz for a 0.3 μm long and 500 μm wide microwave HFET biased in saturation. Lower and upper curves are simulations with and without inclusion of frequency dependence of g_d.

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Heterodimensional MESFETs for Ultra Low Power Electronics

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Introduction

Revolutionary change in electronics technology will be required to meet the pressing need to dramatically reduce the power consumption of large scale integrated circuits in future low power applications such as wireless communications and other portable electronics. Our approach for realizing such change is to utilize novel two-dimensional metal-semiconductor field effect transistors (2-D MESFETs)[1], which not only can be scaled to deep sub-micron dimensions without suffering severe narrow channel and short channel effects [2], but also offer new ways to implement basic logic functions using far fewer transistors than are currently required.[3] In addition to lower power consumption and greater functionality, these new architectures should dramatically simplify the design process and allow much denser packing.

In this paper we present the heterodimensional technology in general and in particular the 2-D MESFET which is one of the devices based on this technology. Furthermore, we explore the advantages of utilizing this device in an integrated circuit environment.

Heterodimensional Technology and the 2-D MESFET

All semiconductor devices utilize interfaces between different regions—ohmic contacts, *p-n* junctions, heterointerfaces and interfaces between a semiconductor and an insulator. Typically, these interfaces are planes separating different regions. Recently, heterodimensional interfaces have been introduced, which utilize interfaces between semiconductor regions of different dimensions. An example of such an interface is a Schottky barrier between a three-dimensional metal (3D) and a two-dimensional (2D) semiconductor as shown in Fig. 1. a). Other heterodimensional Schottky barriers include the 1D-2D contact shown in Fig. 1. b).

The 2-D MESFET is one of the devices based on the heterodimensional technology. This device utilizes sidewall Schottky contacts on either side of a very narrow 2D electron gas channel, as shown in Fig. 2.

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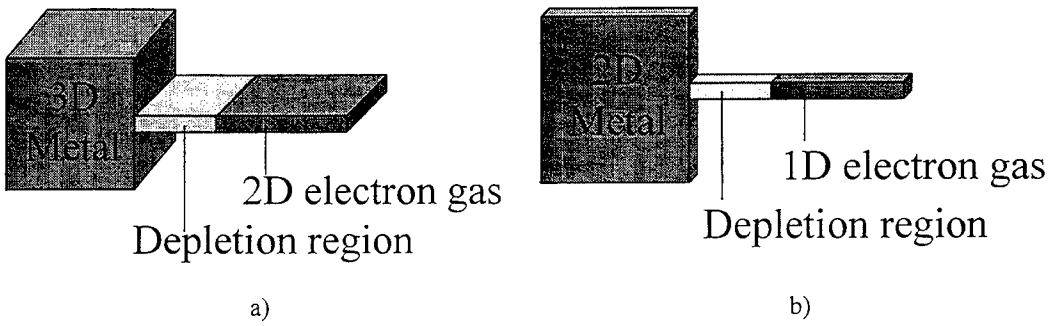

Fig. 1. Heterodimensional Schottky barriers: a) 2D-3D and b) 1D-2D.

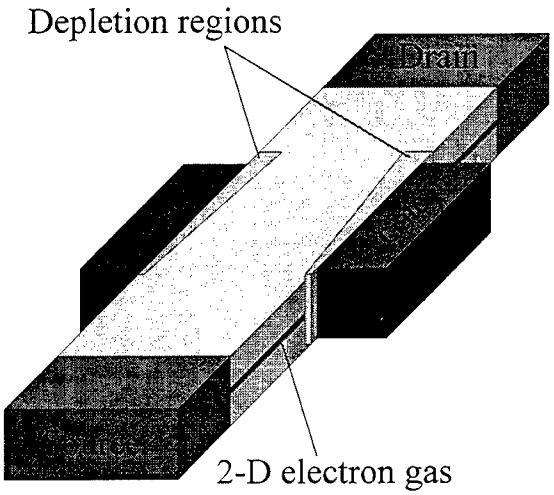

Fig. 2. Perspective illustration of the 2-D MESFET (not drawn to scale).

As we showed in Ref. 1, this gate-channel geometry greatly suppresses effects detrimental to conventional top gate structures such as the Narrow Channel Effect (NCE) and the Drain Induced Barrier Lowering (DIBL). The devices demonstrate excellent scaling characteristics down to submicron dimensions in both the channel length and width.[2] Typical device characteristics are shown in Figs. 3 and 4. A 0.4 micron wide device had an ON/OFF current ratio of 10^5, a peak transconductance of 100 mS/mm, a saturation voltage of 0.2 V, an output conductance less than 1 mS/mm, and a subthreshold ideality factor of 1.1. All these results were measured at room temperature. Ring-oscillator simulations based on measured characteristics predict a power-delay product of less than 0.1 fJ at room temperature, among the lowest power-delay products yet projected for any FET technology.[4]

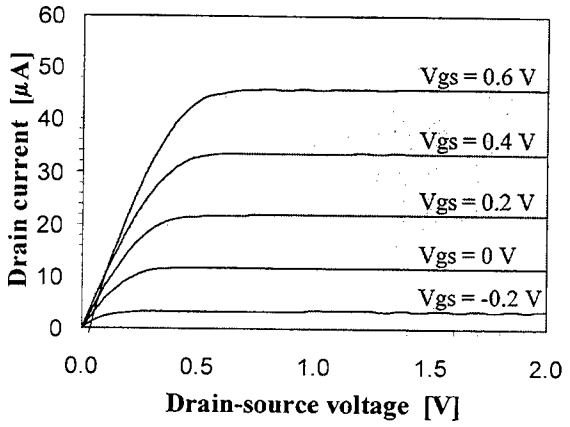

Fig. 3. Measured drain-current versus Vds characteristics of a device with W/L = 0.5μm/0.5μm.

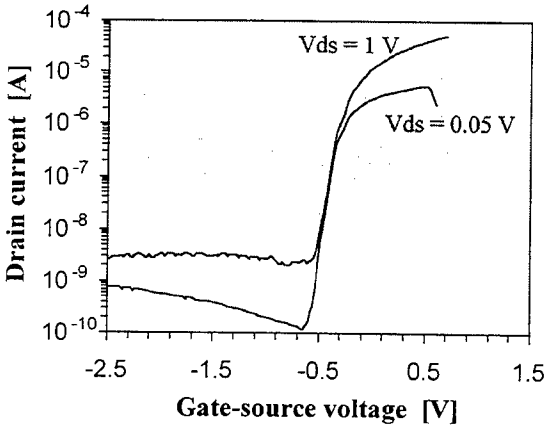

Fig. 4. Measured drain-current versus gate-source voltage characteristics of the same device as in Fig. 3.

High Functionality Digital Gates based on the 2-D MESFET

The greater functionality which is inherent in the two-input 2-D MESFET has already been demonstrated in terms of two-input NOR gates using a single switching device.[3] In Figs. 5 and 6 we show a demonstration of two-input NOR operation using a single 2-D MESFET switching device.

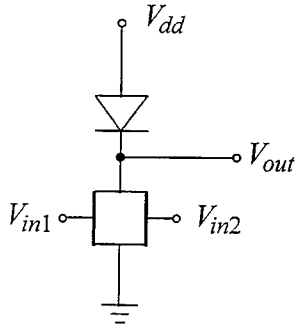

Fig. 5. RTD/2-DMESFET NOR gate using a single switching device.

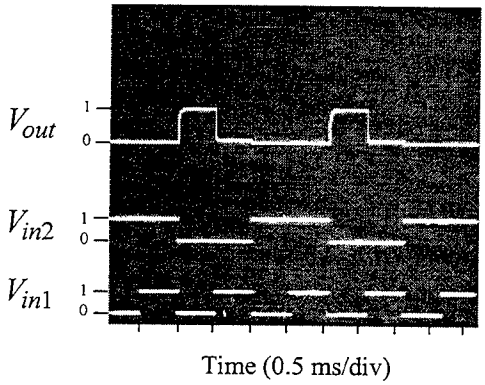

Fig. 6. Measured characteristics of a two-input NOR gate based on the circuit shown in Fig. 5. From Ref. 3.

Based on the same ideas, we have designed and simulated a standard D-type flip-flop (see Fig. 7) utilizing 2-D MESFET DCFL NOR gates using a single switching devices as shown in Fig. 8. The greatest improvement achieved by the 2-D MESFET design is a reduction in required area of 30 times compared to state-of-the-art commercial 0.5 μm MESFET technology.

Furthermore a 33% reduction in the transistor count and an order of magnitude less power consumption are obtained.

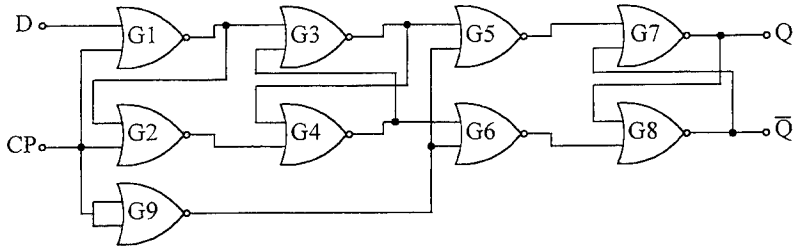

Fig. 7. A standard D-Flip-Flop realized with NOR gates.

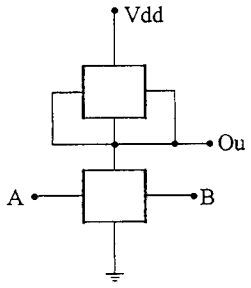

Fig. 8. Two input 2-D MESFET DCFL NOR gate.

Conclusions

We have presented our approach to dramatically reduce the power consumption of future large scale integrated circuits. Our concept is based on the improved functionality and the ultra low power capabilities of the 2-D MESFET, which is one of the devices based on the emerging heterodimensional technology. By utilizing this technology, we have demonstrated simulation results of a D-Flip-Flop implemented in 2-D MESFET DCFL technology. By utilizing the improved functionality and the ultra low power features of the 2-D MESFET, the number of FETs was reduced by 33%, the area was reduced by a factor of 30 and the active power dissipation was reduced by an order of magnitude compared to the design based on conventional state-of-the-art MESFET technology.

Acknowledgments

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UNIFIED C_∞-CONTINUOUS MODELING OF SURFACE-CHANNEL FETs

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Abstract

We present in this paper an original approach to the modeling of surface-channel FETs which leads to complete models valid for all operating regimes. Using a unified charge control model we obtain analytical expressions for the channel current and total terminal charges. By including short-channel effects using appropriate physically-based equations the new technique is extended to deep submicron devices. All equations have an infinite order of continuity; this is very useful in analog design, where accurate expressions of the derivatives of current and charges are needed.

.1-INTRODUCTION.

As surface-channel FETs are scaled down towards the deep-submicron range many physical effects that were negligible in longer devices become relevant. This results in an increase on the complexity of the models, and besides, it can worsen the smoothness of the model because the submicron effects have to be accounted for in a different way in each operating regime. As a result, the models addressed to deep-submicron transistors have a very limited order of continuity that leads to inaccurate values of conductances and capacitances in the transirtion regimes, and convergence problems when applied in circuit simulation.

The modeling technique we propose allows to obtain unified and explicit expressions for all large and small signal parameters. This new technique has been applied to bulk MOSFETs [1], [2], and FD SOI MOSFETs [3]. In this work we extend its application to all surface-channel FETs, and its validity to deep-submicron devices.

2-CHANNEL CURRENT MODEL.

Following a generalized charge-sheet model the channel charge density (q_n), can be written as a linear function of the surface potential, (ψ_s):

$$q_n = -c_{in}\left(V_G - V_{tg} - \alpha\psi_s\right), \tag{1}$$

where V_G is the gate voltage, c_{in} is the capacitance per unit area of the insulator between gate and channel and V_{tg} and α depend on the applied voltages in different ways for the different devices. The former relationship is obtained for bulk MOSFETs by linearizing the term $\sqrt{\psi_s}$ in the charge control equation, but it is exact for FD SOI (where conduction only takes place on the front surface), and for HFETs [1] [5] [4]:

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By considering an appropriate relationship between the carrier velocity and the lateral electric field, and using the drift-diffusion formulation and the gradual channel approximation the channel current is finally written as a function of the channel charge densities at the source and drain ends, $q_{n,s}$ and $q_{n,d}$ [1]:

$$I_{ds} = \frac{W}{L_{eff}} \frac{\mu_n}{1 + (q_{n,d} - q_{n,s}) \frac{\mu_n}{\alpha c_{in} L_{eff} v_{sat}}} \left[v_T (q_{n,d} - q_{n,s}) - \frac{1}{2\alpha c_{in}} (q_{n,d}^2 - q_{n,s}^2) \right], \quad (2)$$

where $L_{eff} = L - l_{sat}$, l_{sat} being the channel length modulation, μ_n is the effective mobility by accounting for the effect of normal fields and κ is a parameter that controls the velocity-field relationship. The mobility degradation model for bulk MOSFETs used in [1], [2] and in [3] for FD SOI MOSFETs, was based on the following relationship between the effective mobility and the normal effective field in the inversion layer:

$$\mu_n = \frac{\mu_0}{1 + \theta t_{in} E_{n,eff} + a_R} \quad (3)$$

where μ_0 is the zero-bias mobility, t_{in} is the insulator thickness and a_R accounts for the effect of series resistances up to first order.

This expression does not work in deep submicron technologies, where the oxide is very thin and therefore mobility degradation is more important. Although (3) can be applied in submicron devices with appropriate parameter values, it becomes necessary to change these values to extend it to longer devices. We have obtained good results for a wide range of channel lengths using a model based on the following relationship between μ_n and $E_{n,eff}$:

$$\mu_n = \frac{\mu_0}{1 + \theta_1 t_{in} E_{n,eff} + \theta_2 t_{in}^2 E_{n,eff}^2 + a_R} \quad (4)$$

In our unified model we define $E_{n,eff}$ as the average effective normal field in the channel and we use our unified models for $q_{n,s}$ and $q_{n,d}$, and the expressions of q_b at drain and source in strong inversion, because mobility degradation is only important in that regime.

For bulk MOSFETs, $E_{n,eff} = -\frac{q_n + 2q_b}{2\epsilon_s}$, where q_b is the depletion charge density. Therefore $E_{n,eff} = \frac{q_{n,s}+q_{n,d}}{2c_{in}} + 2\gamma(\sqrt{2\phi_F + V_{SB}} + \sqrt{\phi_B + V_{SB} + V_{DSE}})$ where V_{DSE} is defined as the value of the effective drain-to-source potential, and γ is the body effect parameter.

The model becomes explicit using unified expressions of $q_{n,s}$ and $q_{n,d}$. The latter will depend on the velocity-field relationship used, which determines the saturation point. Useful expressions of $q_{n,s}$ and $q_{n,d}$, as well as of V_{DSE} were presented in [2].

Using a quasi-two dimensional analysis in the saturated region of the channel we find an expression for l_{sat}, which is continuous and tends to 0 in the triode regime [1] [2]: The effects of charge-sharing and DIBL are included in the expression of the threshold voltage.

3-CHARGE MODEL

By integrating the charge densities we can obtain expressions for the total terminal charges in terms of the applied voltages and the inversion charge densities.

The total intrinsic channel charge can be written as:

$$Q_N = \left[W L_{eff} \frac{v_{Te}(q_{n,s} + q_{n,d})/2 - (q_{n,s}^2 + q_{n,s} q_{n,d} + q_{n,d}^2)/(3c_{ox})}{c_{in} v_{Te} - (q_{n,s} + q_{n,d})/2} \right] + l_{sat} W q_{n,d}, \quad (5)$$

where $v_{Te} = v_T - \frac{I_{ds}}{\kappa v_{sat} c_{in} W \alpha}$

To obtain the total drain and source charges we follow the Ward's channel charge partitioning scheme [1] and we get:

$$Q_D = W(L_{eff}^2/L)\left[\frac{c_{in} v_T \alpha}{2} + \frac{2}{15}\frac{2q_{es}^3 + 4q_{es}^2 q_{ed} + 6q_{es}q_{ed}^2 + 3q_{ed}^2}{(q_{es}+q_{ed})^2}\right] + \frac{W(l_{sat})^2 q_{n,d}}{2L}, \quad (6)$$

where $q_{ed} = q_{n,d} - c_{in}\alpha v_{Te}$ and $q_{es} = q_{n,s} - c_{in}\alpha v_{Te}$

In MOSFETs there is also a depletion charge. In a FD SOI MOSFET the depletion charge density is constant in the whole film. In bulk-MOSFETs the depletion charge density at a point of the channel depends on the applied voltages and on the inversion charge density at that point. Our unified model for the depletion charge in a bulk MOSFET was explained in [2]. The total gate charge in a bulk MOSFETs is obtained from the charge conservation equation. In an HFET the gate charge is equal to $-Q_N$. In a FD SOI MOSFET we have to consider the charges of the front and the back gates [3].

The intrinsic capacitances are obtained by differentiating total charges with respect to the applied bias:

4-RESULTS.

In previous work [1] [2] we shown that our bulk MOSFET model was valid for transistors of channel lengths down to 1.0 μm. The unified FD SOI MOSFET model was also validated for the same range of channel lengths [3].

We have now validated our improved bulk MOSFET model by comparison with measurements of effective channel lengths ranging from 0.25 μm to 15 μm. The transistors came from a Lucent Technology process and were measured in Lucent Technologies Spain.

We have checked that for this technology the model fits well the measurements of I_{ds} and transconductance, g_m, provided the improved effective mobility model is used (Figs. 1-4). It should be remarked that to properly extract the mobility degradation parameters, θ_1 and θ_2 measurements of submicron and long-channel transistors are equally necessary.

5-CONCLUSIONS.

In this work we have presented new unified models for surface-channel FETs. These models are based on using single-piece explicit expressions for the channel charge densities, valid for all operating regimes. The new modeling principles allow to develop a charge conserving model which is consistent with the channel current model. The bulk-MOSFET model has been validated by comparison with measurements of transistors with effective channel lengths down to the quarter-micron range , but since the main short-channel effects have been properly included, it is expected than in general the new modeling technique will be valid for all surface-channel FETs down to the submicron range.

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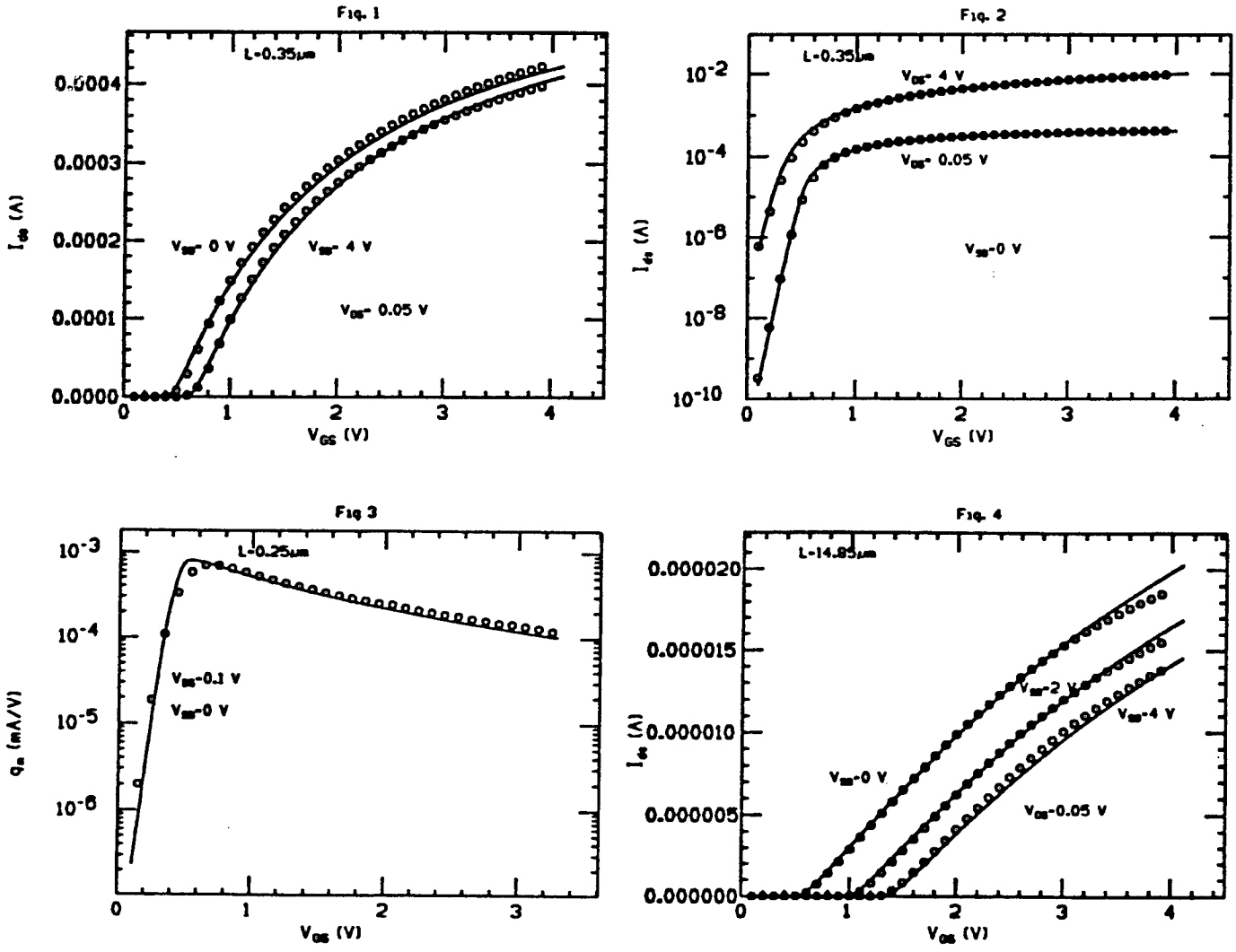

Figs 1-4 Comparison of the measured (symbols) and modeled (solid lines) characteristics of bulk MOSFETs of different channel lengths. For all transistors $W = 15\mu m$.

Ultrafast Circuits and Systems Using Quantum Devices

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1 Introduction

In this paper, we discuss circuit design methodologies and simulation techniques for ultrafast digital systems using resonant tunneling devices. State of the art circuit techniques and process technologies are limited by the incremental performance improvement offered by device scaling. To achieve an order of magnitude improvement in circuit performance, it is necessary to develop technologies that are not solely dependent on device scaling for performance enhancement. Quantum effect devices use a radically different tunneling transport mechanism which allows picosecond device switching speeds and hence quantum circuit technology is a promising emerging alternative VLSI circuit technology. In a concentrated effort in the area of ultrafast circuit design using resonant tunneling devices, at the University of Michigan, we have developed circuit theory, logic families, architectural techniques, and CAD tools for the design of high performance circuit systems using quantum effect resonant tunneling diodes (RTDs) in conjunction with hetero-junction bipolar transistors (HBTs), high electron mobility transistors (HEMTs) and CMOS devices. Figure 1 illustrates various quantum circuit activities being pursued at the University of Michigan in collaboration with several industrial partners. Some of the achievements in this project are shown in Table 1.

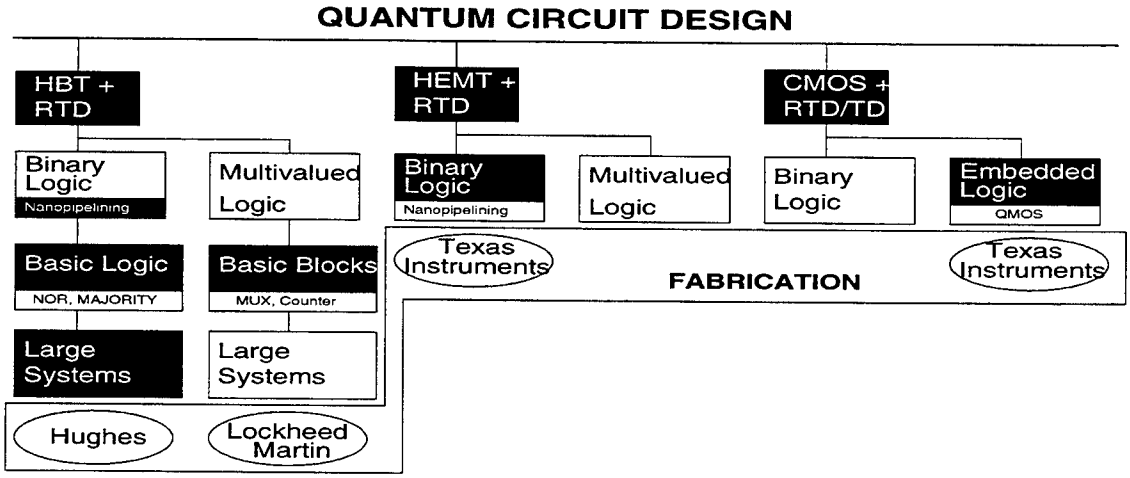

Figure 1: University of Michigan RTD Circuit Activities Overview

2 Quantum Circuit and System Design Activities

Digital circuit applications of RTDs have been exploited to create extremely fast and compact circuits. The self-latching nature of these basic gates has spawned an architectural technique called nanopipelining that achieves gate level pipelining without the area/delay overheads associated with pipeline latches in conventional architectures. More recently, device fabrication techniques for multi-peak RTDs have been developed which have led to implementation of compact multi-state memories and multi-valued logic (MVL) circuits. In this section, we discuss various circuit and system design activities using quantum devices.

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Table 1: Research in Resonant Tunneling Devices at the University of Michigan

Modeling	*Self-consistent device modeling technique and quantum device simulator:* Our scheme takes into account the device contacts in modeling the RTTs with the **Thomas-Fermi** approximation. Applicable to RTTs, RTDs, and RHETs, the accuracy is being improved by taking into account phonon scattering.
Fabrication	We have fabricated several types of **RTDs** with high PVR and high peak current density. PVRs of 24 at 300K and 52 at 77K have been measured in pseudomorphic $In_{0.53}GaAs/AlAs$ RTDs. Designed, fabricated and demonstrated **BSRTTs** for the first time. We have fabricated InGaAs/AlAs/InP **RHETs** with DC gain of 5 and PVR of 4 at 77K.
Simulation	An NDR circuit simulator which performs DC and transient analyses.
Digital Circuits	**Multi-state memory** and **multiple-valued logic** circuits using RTDs. Statistical circuit optimization tool and interconnect delay estimation tool have been designed. BSRTTs and RHETs have been used to design **compact self-latching logic** circuits. An ultra-fast pipelined adder has been designed and simulated using BSRTTs. A 32-bit correlator has been designed to operate at 12 GHz and it employs only 2000 devices as opposed to 6000 CMOS transistors. 4-valued mux, demux, analog selector and programmable gate-array have been designed. Q-MOS basic gates, adder, and correlator have been designed.

2.1 RTD-HBT, RTD-HEMT, RTT and quantum MOS Digital Circuits

We have developed quantum circuits based on resonant tunneling devices that are useful for implementing high-throughput, deeply pipelined digital systems. The folded characteristic of an RTD makes it a useful load device which when properly biased, draws very low currents for both high and low outputs.

Bistable Logic Gates: Self-latching NAND, NOR and MAJORITY gates have been designed using RTD-HBT, RTD-HEMT and RTT logic families. These gates have been used in the implementation of a nanopipelined full adder, illustrated in Figure 2a that operates on a two-phase clock and allows two computations to be concurrently active, thus improving the system throughput. We have developed a logic family using RTDs and CMOS devices that achieves compact, self latching digital gates and alleviates charge sharing problems associated with dynamic CMOS while also improving circuit power-delay product.

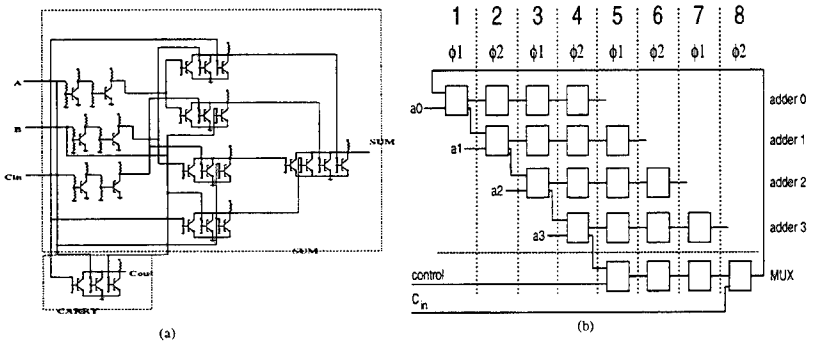

Figure 2: (a) Bistable full adder (b) Nanopipelined addition scheme

Nanopipelined 64-bit Adder: Four 1-bit nanopipelined adders are connected in a ripple carry fashion, with the output of the last bit being fed-back to the first bit in a controlled fashion to perform 64-bit addition. The addition scheme is illustrated in Figure 2b. Using just four full adders, 64-bit addition is accomplished in 1 ns.

32-bit Parallel Correlator: High throughput CDMA systems that use long PN sequences require very high-speed parallel correlators. We have designed an RTD-HBT based 32-bit correlator consisting of a nanopipelined adder network, illustrated in Figure 3a, that can provide an effective throughput of one 32-bit correlation every 100 ps with a power dissipation of 1.5 W. The circuit uses only 2000 devices as compared to 6000 devices in a conventional CMOS correlator, and offers a tenfold improvement in the power-delay product.

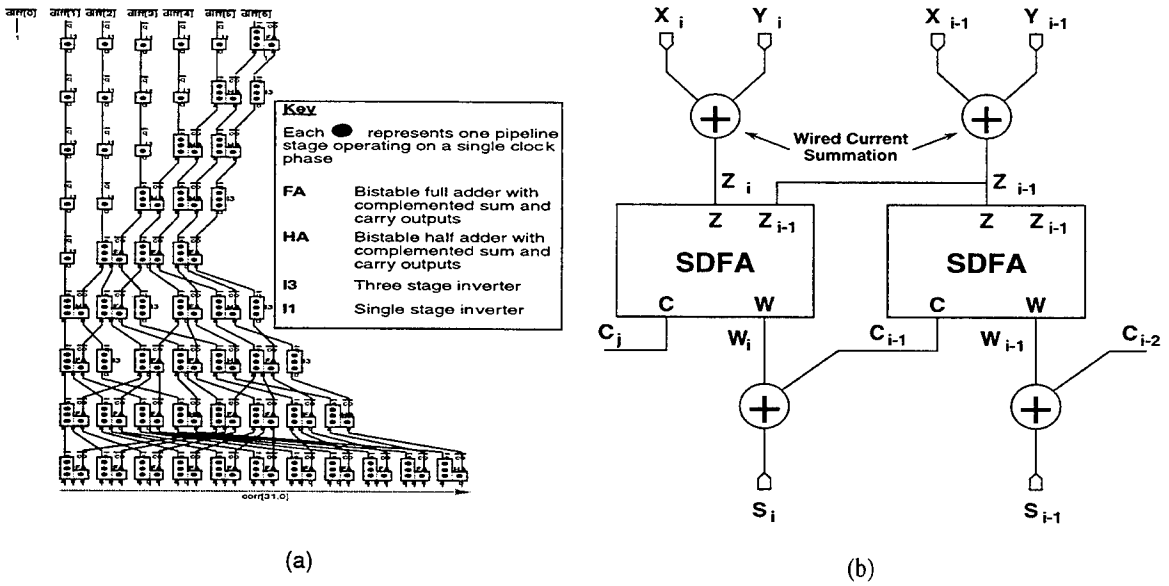

Figure 3: (a) 32-bit pipelined adder network (b) Signed-digit full-adder block diagram

2.2 RTD-based Multiple-valued Logic

Multiple-valued logic (MVL) technique decreases interconnect complexity while also reducing the number of building blocks in system designs. However, implementation of MVL systems using conventional technologies such as CMOS has yet to provide a viable alternative to binary logic because individual MVL blocks have high device counts and low speeds. The advent of multiple-peak resonant tunneling diodes (MPRTDs) facilitates compact and high-speed MVL circuit implementation due to the multiple-folded nature of the I-V characteristics and picosecond switching speed of MPRTDs.

Signed-digit Full-adder: A signed-digit adder based on a combination of RTD and CMOS devices has been designed. This design, shown in Figure 3b, uses *current-mode* signal representation which allows *wired addition* of signals. The adder implements radix-2, signed-digit addition, and hence requires a three-level logic (using digits $\{-1, 0, +1\}$). This new signed-digit adder uses 13 MOS transistors, while 44 transistors are used in an equivalent redundant-binary static CMOS implementation. The SDFA circuit finds use in embedded computing subsystems such as a fast multiplier for high performance microprocessors. We have designed, fabricated and tested a prototype 7x7 parallel multiplier in CMOS which uses redundant signed digit arithmetic. Efforts are currently underway to cointegrate RTDs with MOS devices in order to increase compactness and improve the speed of operation of the multiplier.

4:1 Four-valued Multiplexer: A 4:1 four-valued multiplexer has been designed using RTDs and HBTs. It uses a RTD ladder selector switch along with HBT current mirrors to implement the said function using only 21 HBTs and 4 RTDs. The use of high performance HBTs also enables the same circuit to operate as an analog selector switch. A 4-valued staircase function is used to select one of four 4-valued inputs to be available at the output of the multiplexer. The 4:1 multiplexer, shown in Figure 4a, has a power dissipation of 310 mW while operating at a speed of 500 MHz.

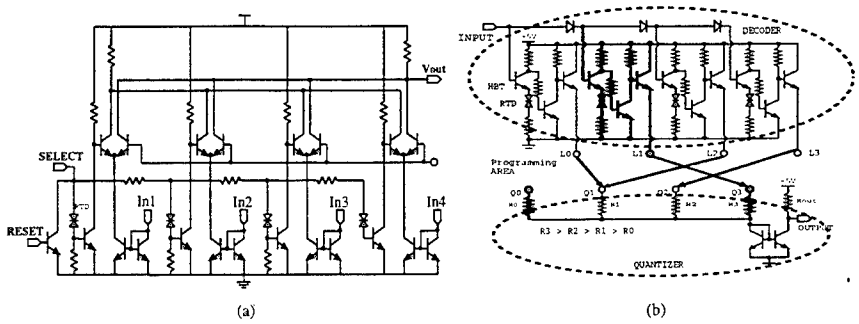

Figure 4: (a)RTD-HBT 4:1 multi-valued multiplexer (b) RTD-HBT MVL gate array

MVL Gate Array: We have designed a literal generator using 1 RTD and 3 HBTs that forms the basis of a mask-programmable MVL gate array, illustrated in Figure 4b. Using programmable interconnects, we are able to implement any number of multi-valued boolean functions. Both one- and two-input 4-valued gate arrays have been designed. They use a binary decoder at the input whose decoded outputs are used by a quantizer to generate the multi-valued output. A two-input 4-valued MVL gate array operates at 400 MHz.

Table 2 summarizes our circuit design achievements using quantum devices.

Table 2: Summary of self-latching quantum circuits

Circuit	Technology	Power	Speed/Delay	Noise Margins
And3	RTBT	10mW	40ps	0.3V
Or3		10mW	37ps	0.3V
Carry		10mW	34ps	0.3V
Nor3	RTD-HEMT	0.48mW	5GHz	IH=90mA, IL=0
Minority		0.6mW	(25GHz max)	NMH=17mA
Nand3	(dep)			NML=9mA
Nor3	RTD-HEMT	0.3mW	5GHz	same as above
Minority	(enh)		(25GHz max)	
Nor3	RTD-HBT	0.5mW	25GHz	0.3V
Minority				
Majority	QMOS	0.1mW	200ps	0.5V
Full Adder		0.4mW	2.5GHz	
T-gate	RTD-HBT	327mW	2.87ns	0.3V
		3.2mW	33.3ns	
MVL Gate Array		500mW	2GHz	
32-b Adder	RTD-HBT	10mW	560ps	
32-b Correlator	RTD-HBT	1.5W	10GHz	
	RTD-HEMT	1W	3GHz	
	QMOS	0.6W	2.5GHz	

3 CAD Tools for Quantum Circuits

We have developed several CAD tools to simulate and optimize quantum circuits. Following is a summary of our research work in this area.

3.1 Simulation of Quantum Circuits

In the device design stage, a device simulator which solves the Schrödinger and Poisson equations self-consistently, including phonon scattering effects, is used to obtain the most desirable I-V characteristics for the device. The resulting I-V characteristics are then used in a circuit simulator to simulate quantum circuits. We have developed a quantum circuit simulator called NDR-SPICE, incorporating device specific convergence routines, which can overcome many of the convergence problems that SPICE-like circuit simulators face while dealing with negative differential resistance devices. This simulator has enabled us to simulate many previously hard-to-simulate quantum circuits.

Even though NDR-SPICE in its current form is good enough for most circuits, we have found that it is not very efficient for large circuits. Also, this simulator was built around a piece-wise linear model of resonant tunneling devices and as such is not very accurate. We intend to use artificial parameter homotopy based methods on simple quantum device models and then use the dc operating point thus derived as an initial guess of a circuit simulator which uses accurate physics based NDR device models that have been recently proposed (e.g., by Dr. Chow's group, Hughes Research Laboratories). Apart from dc convergence problems, we find that a number of RTD based circuits can also cause convergence problems in simulators during transient analysis. Unlike conventional circuits, the nodal equations of quantum circuits can have more than one solution and this number can undergo a sudden change with time. This can be a major problem when simulating circuits which undergo transition from monostable to bistable mode. We are at present investigating several such problems and are developing specific routines to handle each of them.

At high frequencies of operation, the interconnects play a crucial role in determining circuit performance. It is not always possible to incorporate the interconnect delays right at the time of circuit simulation, since the layout and processing information are not readily available at that stage and as such, the simulation results are always too optimistic. We have developed a simple Delay Estimator tool which is capable of projecting a more realistic circuit performance than that offered by circuit simulators alone. From the SPICE description of a circuit, the Delay Estimator determines the number of terminals that need to be connected. By using Rent's rule, it estimates the interconnect length distribution in the circuit and represents these interconnects by means of various models. The resulting augmented circuit is then simulated to obtain a realistic picture of the performance of the circuit.

3.2 Optimization of Quantum Circuits

We have proposed an optimization technique for RTD-based circuits that maximizes design tolerances and minimizes power dissipation, based on a modified simplex method. The optimization scheme is well applicable to all self-latching circuits and also to multiple-state memory design. The key features of the optimization technique are: a) Switching conditions are described by linear in-equations in the line currents and the RTD peak/valley currents; b) A graph-based technique is used to derive the relationships between all the constraints and extract a minimal set of non-redundant constraints; c) Objective functions can either be a continuous function of the currents such as power consumption, or a min-max function on the margins. Since these objective functions are not all linear in the input variables, non-linear optimization techniques must be used. In particular, a methodical search in margin space using Multiple Linear Programming approach, has been successful in initial attempts at solving this problem.

We have derived analytical expressions describing delay, power dissipation and noise margins for circuits built with quantum devices in conjunction with CMOS or HBTs. These equations are extremely complex and unwieldy in nature and will require sophisticated numerical methods to solve in order to find optimal design points. Hence we are developing a statistical optimization tool based on Response Surface Methodology. Starting from a nominal design of a circuit, this tool will perform a parameter space sampling and then fit a Response Surface to model the objective function. Global optimization methods will be used on this function to determine the optimal design point. In its present form, the optimization tool uses Latin Hypercube based parameter sampling technique. Thereafter, it uses parameter transformation techniques to obtain an accurate quadratic response surface fit. Finally, global optimization is performed by means of a simulated annealing package and the result is refined by Fractional Factorial technique. We are developing this optimization tool such that it can accurately model the sharp ridges and valleys in the response surfaces which are common to quantum circuits.

4 Acknowledgments

Several past and current graduate students at the University of Michigan have conducted the research presented in this paper. They are: Dr. S. Mohan (currently with Xilinx, Inc.), Eric Chan (currently with Cypress Semiconductor), Mayukh Bhattacharya, Alejandro González and Shriram Kulkarni. This research has been made possible by grants from DARPA and ARO's URI program. Prof. G. I. Haddad and his group at the University of Michigan have fabricated some of the basic RTD-based circuits. Dr. A. Seabaugh at Texas Instruments co-ordinated the fabrication of RTD-HEMT circuits and Dr. D. Chow at Hughes Research Labs was responsible for fabrication of RTD-HBT circuits. Naval Research Laboratory has provided help for developing Silicon-Germanium material systems. Georgia Tech University has made accessible their lift-off technology for co-integrating RTD and CMOS devices.

5 Publications

1. H.-L. E. Chan, M. Bhattacharya, and P. Mazumder, "Mask-Programmable Multiple-Valued Logic Gate using Resonant Tunneling Diodes." *IEE Proceedings—Circuits, Devices and Systems*, vol. 143, No. 5 pp. 289–294, Oct. 1996.
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8. S. Mohan, P. Mazumder, R. K. Mains, J. P. Sun, and G. I. Haddad, "Ultrafast pipelined adders using RTTs," *Electronics Letters*, vol. 27, pp. 830–831, May 1991.
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10. S. Kulkarni, P. Mazumder, and G. I. Haddad, "High-Speed 32-bit parallel correlator for spread spectrum communication," in *Proceedings of the 1996 9th International Conference on VLSI Design*, (Bangalore, India).
11. S. Kulkarni, P. Mazumder, and G. I. Haddad, "A 32-bit ultrafast parallel correlator using resonant tunneling devices," in *Proceedings of the International Conference on Integrated Micro/Nanotechnology for Space Applications*, (Houston, Texas), October 1995.
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STUDY OF SEMICONDUCTOR DEVICES FROM AB INITIO THEORY

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Abstract

We present a study of the atomic and electronic properties of the polar InAs/GaSb (001) interface by means of first principles total energy calculations based on the Density Functional Theory. We investigate the extent to which the fundamental parameters of semiconductor devices, the valence and the conduction band offsets, can by modified by controlling the interface composition an geometry at the heterojunctions. We analyze two different chemical composition (GaAs or InSb) of the interface. Our results shows that depending on the atomic composition at the interface the band lineup can be modified, providing a mechanism for band offset engineering.

1. Introduction

The possibility of controlling the band offset at semiconductor heterojunctions by modifying the local interface environment have attracted much attention in the past ten years [1-5]. Methods to change the band lineups would implicitly clarify the microscopic mechanism that determine the band alignment, and would have a substantial technological impact, because the band discontinuities at the interface are the key parameters of most of novel solid state electronic devices. The valence band offset and the conduction band offset, ΔE_v , ΔE_c , determine the confinement and the transport properties at the interface region, so the possible control and the tunability of these parameters has become a fundamental objective both for technology and basic research.

Recent theoretical developments have show the role of the local atomic dipoles created at the heterojunction interface [1], showing that heterovalent heterojunctions with polar orientation are the most promising candidates for offset tuning through modification of the local interface region [2]. The atomic scale control of the interface composition achieved by deposition of ultrathin layers creates an electronic dipole that shifts the energy band structure of the semiconductor forming the heterojunction. Theoretical studies of Rodríguez-Hernández et al. [6] show how the deposition of thin Ge layers at ZnSe/GaAs heterojunction can modified the band discontinuities. Experimentally the Molecular Beam Epitaxy (MBE) technique can exploit the possibility of achieve different local atomic configurations and different band offset. Recent work of Daily and coworkers [7] shows that in InAs/GaSb (001) heterojunction the band discontinuities can be dependent on the interface chemical composition.

In this work we present results of an ab initio calculation based on the Density Functional Theory , DFT, in the framework of the Local Density Approximation (LDA) to the exchange-correlation energy implemented in a plane waves basis set and a pseudopotential scheme, of the

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valence band offset dependence with the interface chemical and atomic composition for the InAs/GaSb (001) heterojunction. InAs and GaSb semiconductors share no common atom, so both anion and cation change across the interface. Thus it is possible to analyze two different types of interfaces with , in the ideal case, either GaAs or InSb monolayer at the interface region, depending on the order in which the group III and the group V elements are switched during the growth sequence. We analyze the ideal abrupt configuration of both cases and we also analyze the effect of relaxation of the atoms at the interface region.

2. Description of the method

In this section we briefly describe the calculational method employed. In order to evaluate the valence band offset, VBO, we split this magnitude into two contributions: (i) the difference in the averaged total potential (the sum of Hartree, exchange plus correlation, and the local part of the ionic pseudopotential) on the two side of the interface, ΔV_{tot} , and (ii) the difference in the energies of the valence band maximum of the bulk material, ΔE_{VBM} , calculated with respect to the above averaged aligned potentials. The first part can be computed from selfconsistent supercell calculations containing thick slabs while the second part is obtained from separate band structure calculation for the two bulk materials.

The dipole contribution ΔV_{tot} at the interface was calculated by first computing the (x,y) planar average of the selfconsistent potential $V(\vec{r})$,

$$V(z) = \int_{2D-Ws} V(\vec{r}) \, dx \, dy$$

(Where X,Y are orthogonal axes in the (001) plane and the integration is taken over the two dimensional Wigner-Seitz cell) and then computing the one-dimensional average $\overline{V}(z)$ of V(z) over a period centered at z,

$$\overline{V}(z) = \int_{z-T/2}^{z+T/2} V(z') \, dz'$$

All the total energy calculations were performed within the DFT using The Ceperley and Alder [8] form for the exchange-correlation energy in the local density approximation (LDA). A non-local norm-conserving pseudopotential scheme was used and the Khon-Sham equations[9] were solved in the reciprocal space using a plane waves basis set up to a kinetic energy cutoff of 12 Ry ($\cong$ 4000 plane waves). In cases where there is a considerable overlap between the valence and the core orbitals, as the case in In and Ga atoms, one must be careful to treat the exchange-correlation potential properly. The exchange-correlation potential is a nonlinear functional of the charge density and cannot be separated into valence and core contributions, as is normally done in pseudopotential calculations. For the calculations on the InAs/GaSb (0 0 1) system we have included non-linear core exchange-correlation corrections (NLCC) in the In and Ga pseudopotentials, which improve its transferability and has been shown to yield more accurate VBO for heterojunctions [10]. The inclusion of NLCC takes into account the effect of the In and Ga shallow 3d levels. These corrections are included following the ideas of Louie el al. [11]. We

also obtain the forces on the atoms via the Helmann-Feyman theorem and the stress tensor using the Nielsen-Martin theorem.

The supercell method was employed. The interface region was modeled using a periodically repeated slab of 16 atomic (001) zincblende-like layers that is enough to reproduce the bulk-like character at both sides of the interface. In the beginning of the calculation all the atom were assumed at the ideal zincblende positions, because InAs and GaSb have similar lattice constants (6.0583 Å and 6.0958 Å respectively). For the atoms at the interface region, when having GaAs (a=5.6532 Å) or InSb (a=6.4793 Å), an additional strain will appear at the interface region, in this case we allow the atoms at the interface region to relax in the (001) direction, using the information on the forces on the atoms and the stress anisotropy, in order to obtain the most stable interface geometry.

In all the cases studied the reciprocal space integrations were performed using a set of 45 k special points within the irreducible wedge of the Brillouin zone, in order to have well converged results.

3. Results and conclusions

Our results show the effect of GaAs and Insb natural interlayers on the band discontinuities of the InAs/GaSb heterojunction. In Fig.1. we present the average of total potential for the InAs/GaSb (001) heterojunction , for the GaAs chemical interface and for the InSb chemical interface including relaxation of the atoms at the interface. The figures show clearly that the supercell size is enough to reproduce bulk-like character at both sides of the interface region and clearly demonstrate the effect of the chemical composition of the interface on the band offset of the InAs/GaSb (001) heterojunction. Also a difference on the atomic dipole appear when relaxing the interface due to the strain related with the lattice constant mismatch of the GaAs or the InSb interlayer.

We obtain that the relaxed InAs/GaSb(001) heterojunction are more energetically favorable that the ideal ones. For the of relaxed InAs/GaSb (001) we find that the VBO is 0.524 eV for the GaAs-like interface and 0.577 eV for the InSb-like interface, so the InSb-like interface has a VBO 53 meV higher in agreement with recent experimental results [7] and with other theoretical empirical models [12]. In all the case we have included a posteriori the spin- orbit effects for InAs and GaSb. Finally from our study we conclude that the effect of the chemical composition of the interface for the InAs/GaSb (001) heterojunction and the inclusion of the atomic relaxation provide a mechanism for the modification of the band offset in this interface. In conclusion our study shows how ab initio calculations are useful to study semiconductors devices, showing that the band discontinuities depends clearly on the interface geometry and the chemical composition.

Acknowledgements

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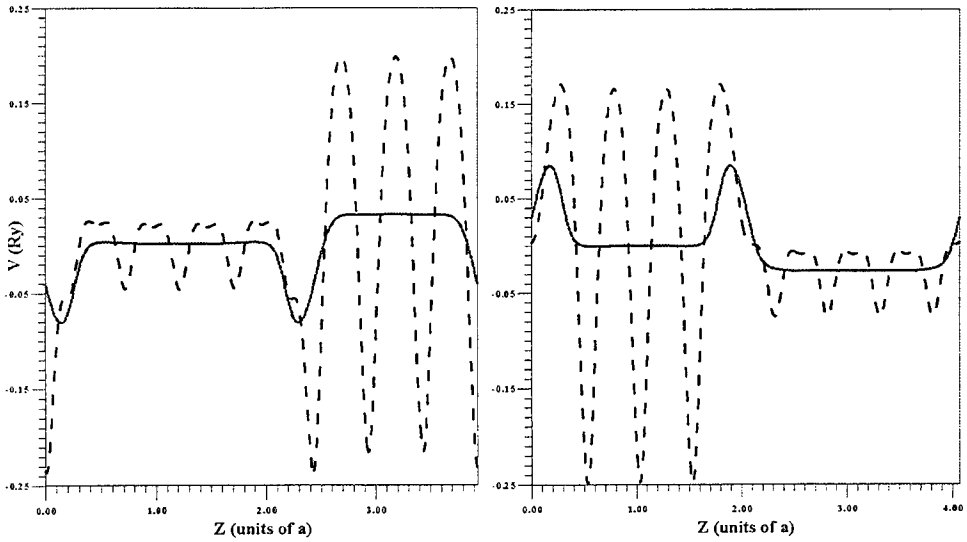

Fig. 1.Electrostatic potential at the InAs/GaSb (001). Dashed line: (x, y) average V(z). Solid line: period average along the (001) direction $\overline{V}(z)$. Left hand side: InAs/GaSb (001) heterojunction with GaAs chemical interface. Right hand side: GaSb/Insb (001) heterojunction with chemical InSb interface.

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Appendix A
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